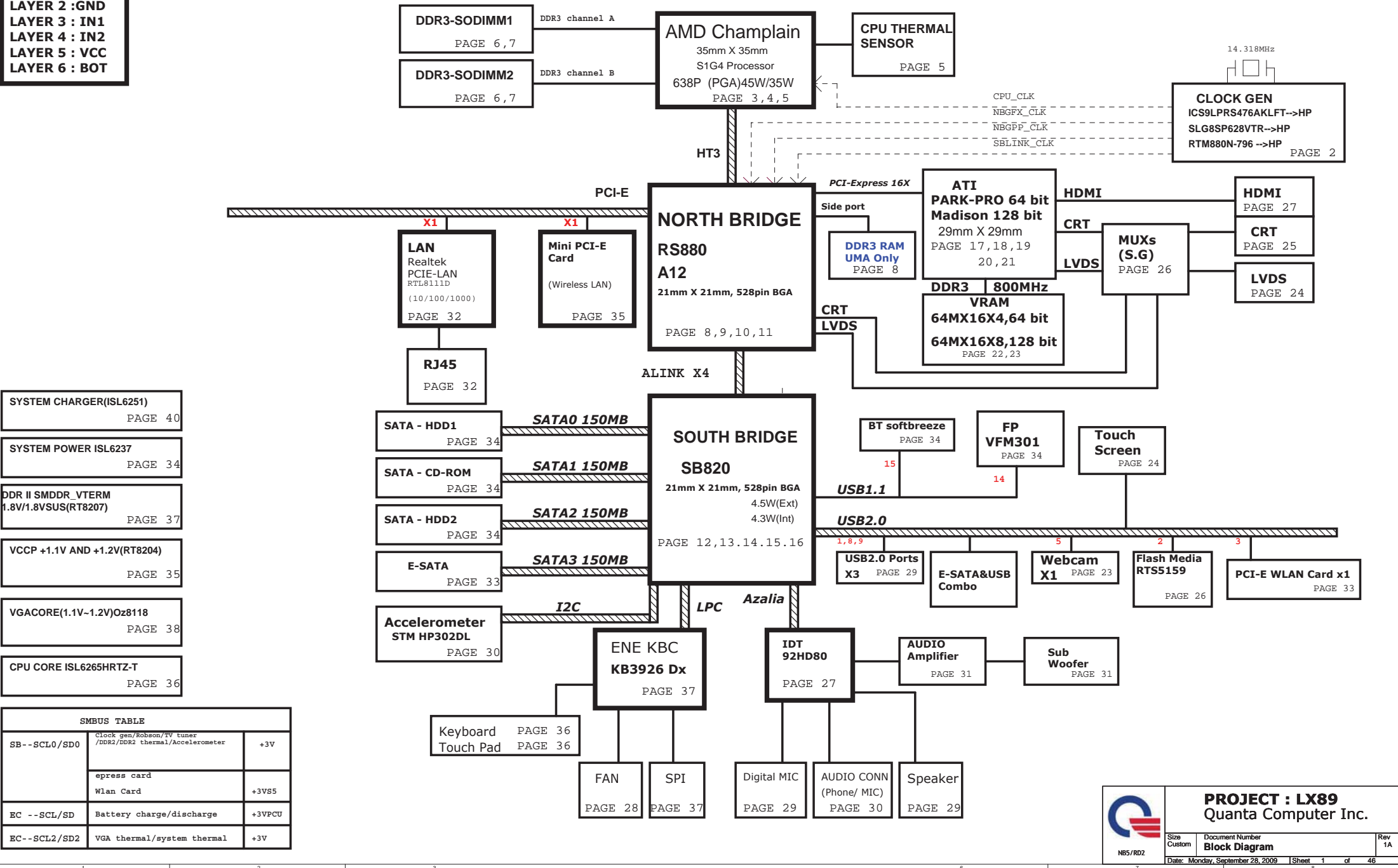


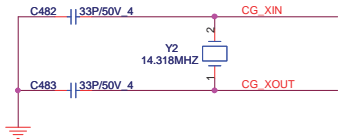
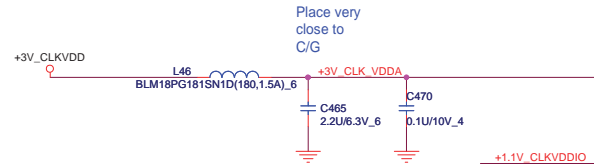
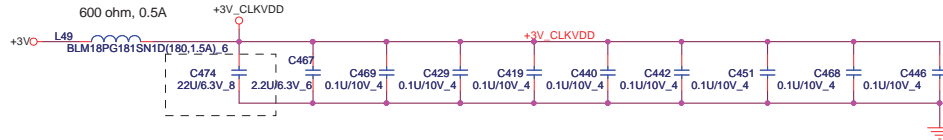
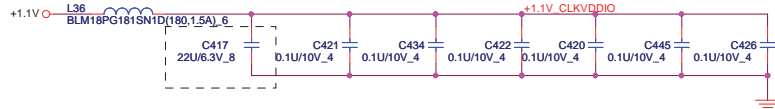
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

LX89 SYSTEM DIAGRAM



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Monday, September 28, 2009 Sheet 1 of 46		



6,7,13,30,34 PCLK_SMB
6,7,13,30,34 PDAT_SMB

PCLK_SMB
PDAT_SMB

CLK_PD#

CLKREQ0#

CLKREQ4#

CLKREQ3#

CLKREQ2#

CLKREQ1#

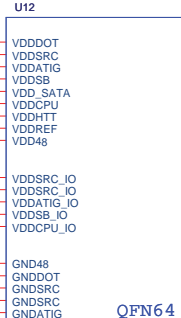
CLKREQ0#

CLKREQ2#

CLKREQ3#

CLKREQ4#

if use clock
request pin, need
to pull Hi for
default setting



QFN64

X1
X2

SMBCLK
SMBDAT

PD#

CLKREQ0#

CLKREQ4#

CLKREQ3#

CLKREQ2#

CLKREQ1#

CLKREQ0#

CLKREQ2#

CLKREQ3#

CLKREQ4#

CLKREQ0#

CLKREQ2#

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CLKREQ3#

CLKREQ4#

CLKREQ0#

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CLKREQ4#

CLKREQ0#

CLKREQ2#

CLKREQ3#

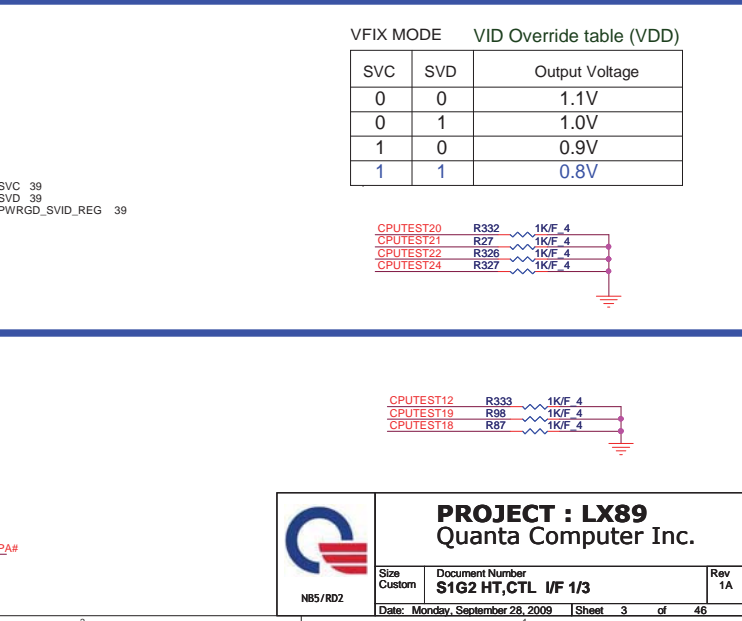
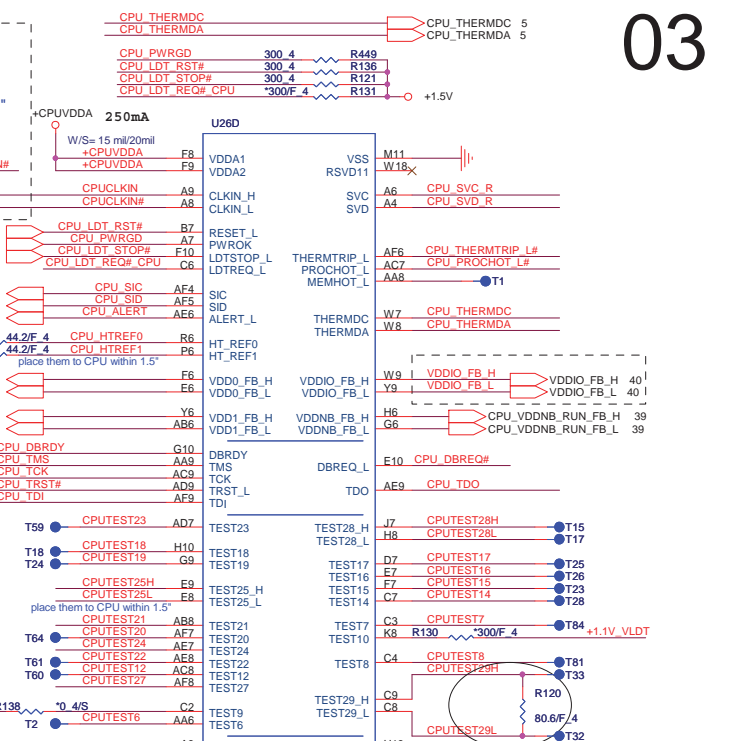
CLKREQ4#

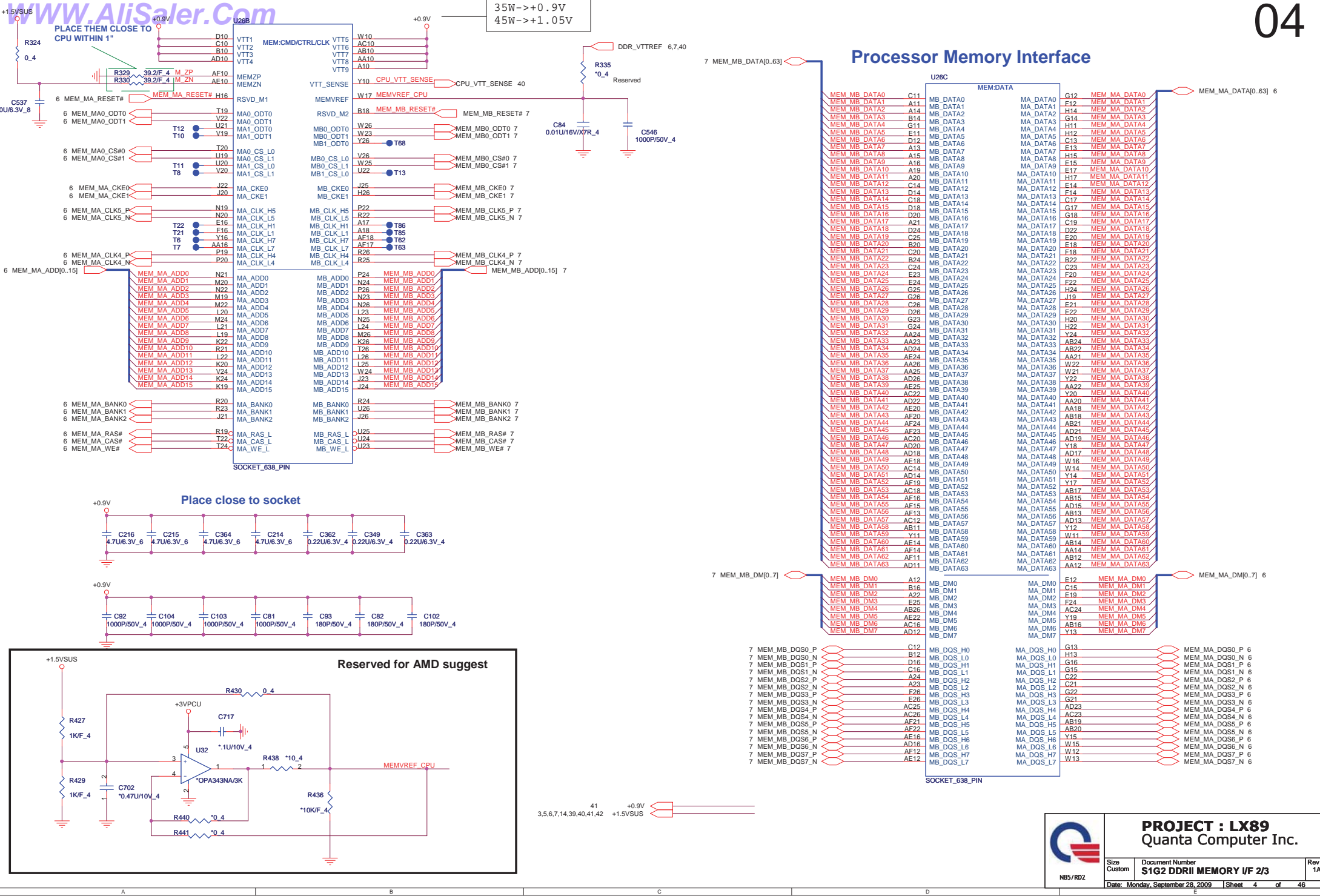
CLKREQ0#

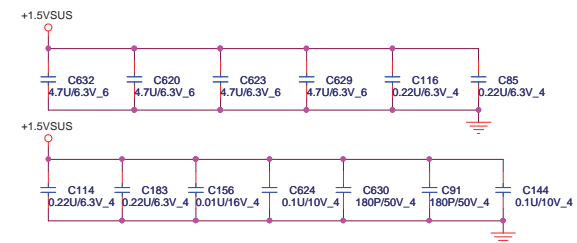
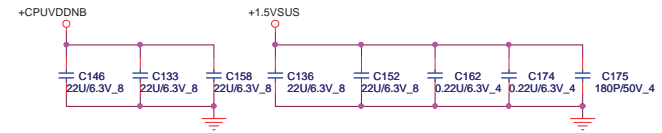
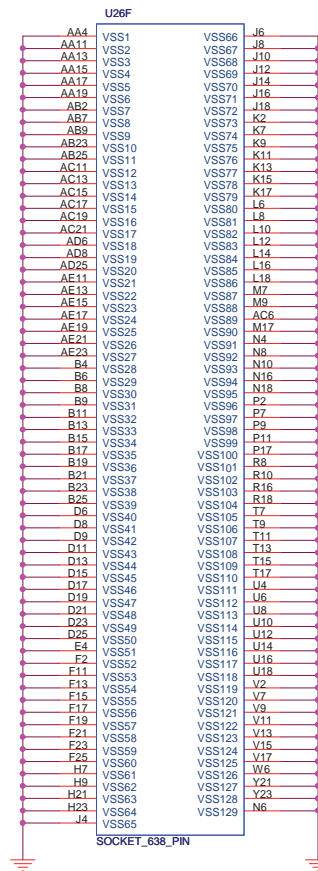
CLKREQ2#

CLKREQ3#

CLKREQ4#







reserve for power shutdown
(if can)

37 SYS_SHDN#

36 3920_RST#

16,36 ECPWROK

+3V

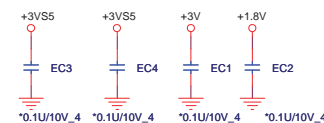
19 TEMP_FAIL

ADD VGA TEMP_FAIL function
M92 is active Hi

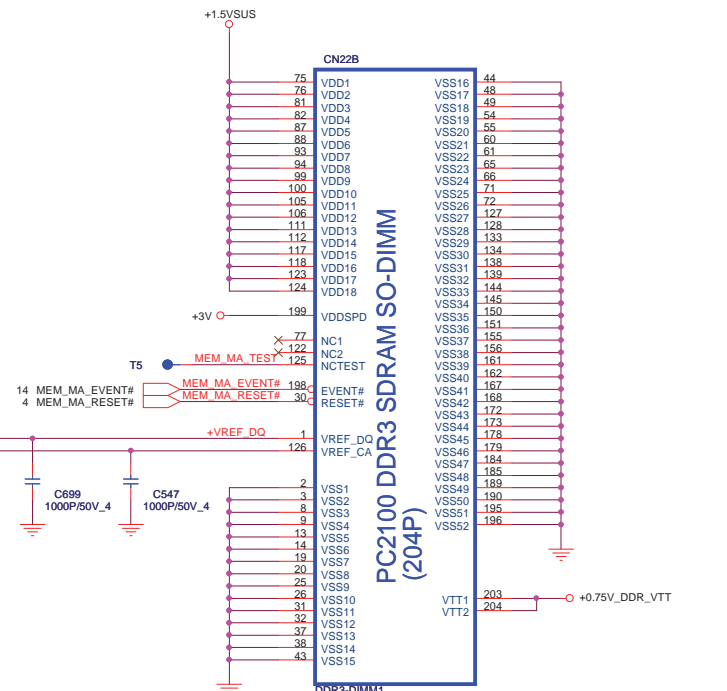
+3V5 EC3

+3V

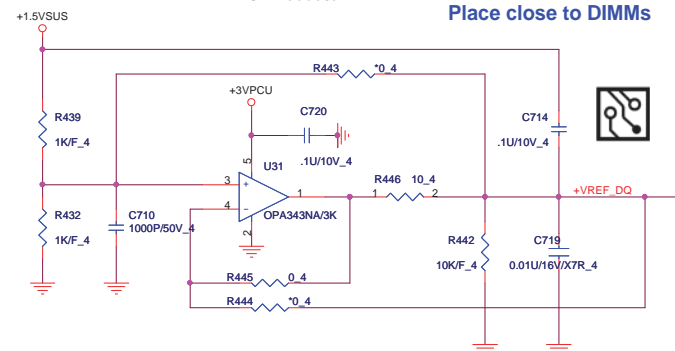
For fix HyperTransport nets
across plane splits



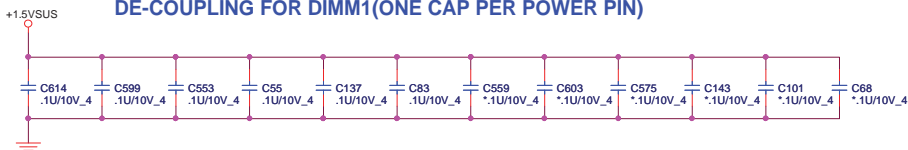
Size Custom	Document Number S1G2 PWR & GND 3/3	Rev 1A
Date: Monday, September 28, 2009		Sheet 5 of 46



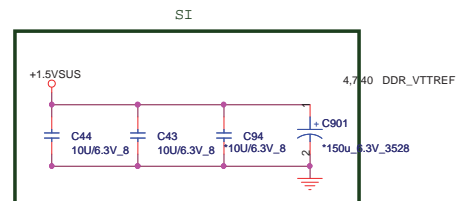
Place close to DIMMs




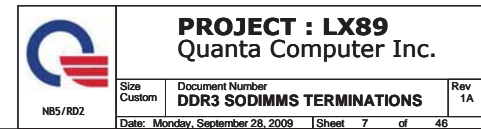
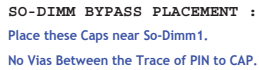
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

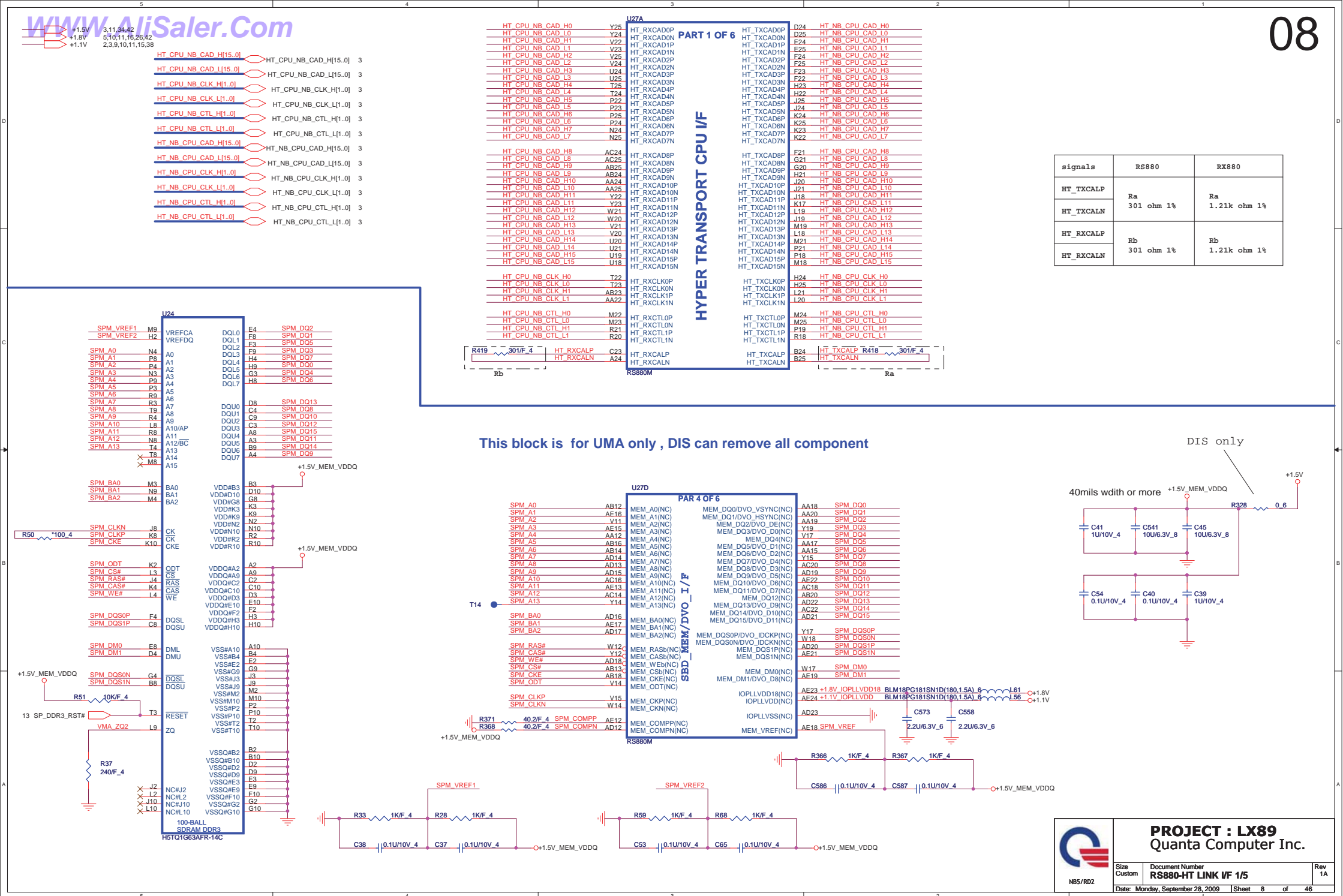


DE-COUPLING FOR DIMM1



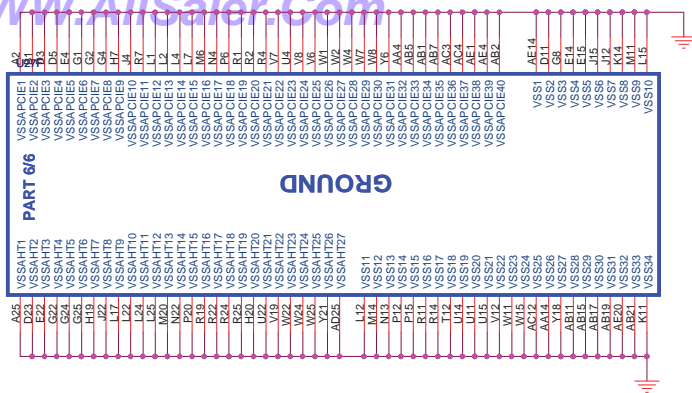
 NBS/RDZ	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number DDR3 SODIMMS: A/B CHANNEL	Rev 1A
Date: Monday, September 28, 2009		Sheet 6 of 46	





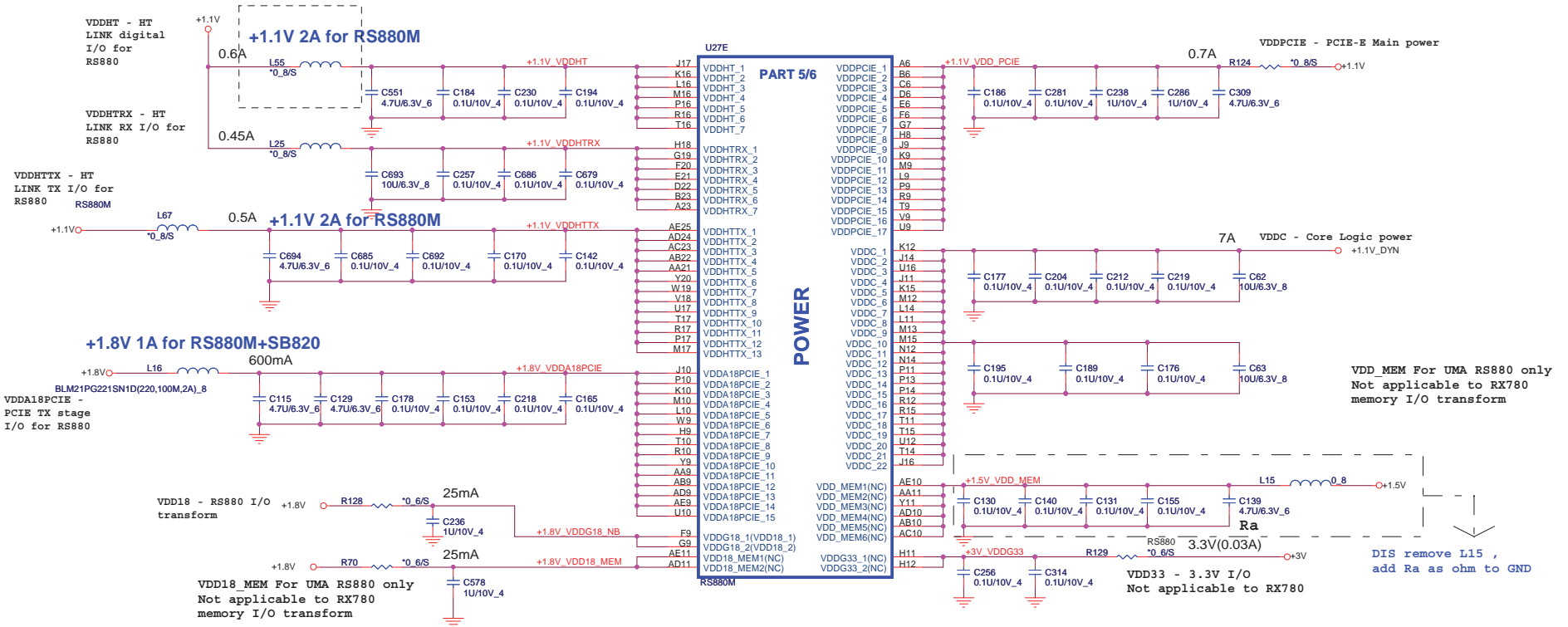


DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

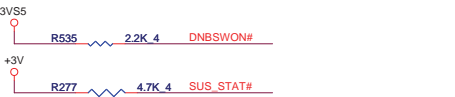
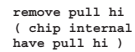
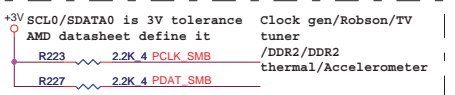


RS880M POWER TABLE

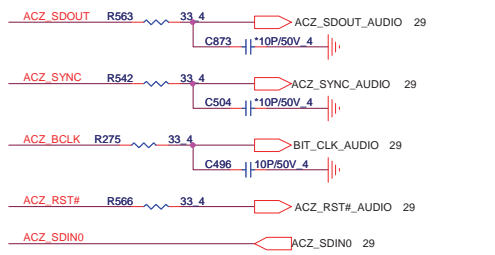
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



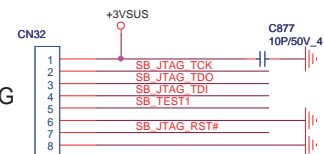
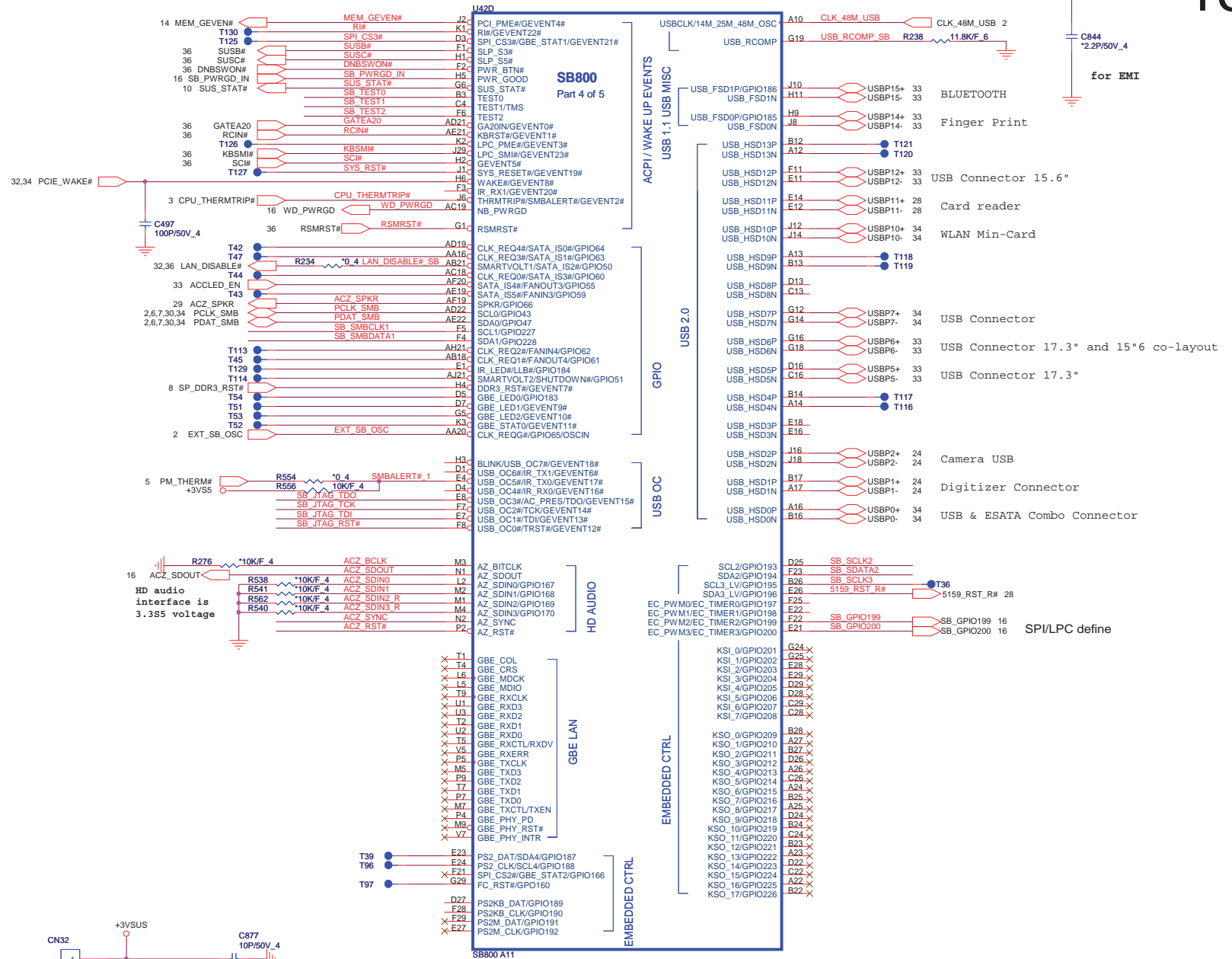





To Azalia



*S/W JTAG DEBUG



 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number SB820-ACP/GPIO/USB 2/4	Rev 1A
Date: Monday, September 28, 2009		Sheet 13 of 46	

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

+1.1V_AVDD_SATA 15
+3V 2,3,5,6,7,10,11,12,13,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V5 5,12,13,15,16,42

SATA1 HDD

SATA ODD

SATA2 HDD

E-SATA



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL. 4.99K 1% FOR 100MHz
INTERNAL CLOCK

XTLVDD SATA-- SATA
crystal power

PLVDD SATA--
SATA PLL
POWER

+1.1V_AVDD_SATA

SB_SATA_LED#

AD11

SATA_X1

AD16

SATA_X2

AC16

+3V

R271

10K/F 4

AD11

SATA_X1

AD16

SATA_X2

AC16

220/50V 4

C820

Y6

25MHZ

1M/F 4

R491

AD16

AC16

220/50V 4

C812

SI

Remove Y6 for AMD recommend

AD11

SATA_X1

AD16

SATA_X2

AC16

+3V

R271

10K/F 4

AD11

SATA_X1

AD16

SATA_X2

AC16

220/50V 4

C820

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25MHZ

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220/50V 4

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SI

Remove Y6 for AMD recommend

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SATA_X1

AD16

SATA_X2

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220/50V 4

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220/50V 4

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AC16

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C820

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AD16

SATA_X2

AC16

220/50V 4

C820

Y6

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AD16

AC16

220/50V 4

C812

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SATA_X1

AD16

SATA_X2

AC16

220/50V 4

C820

Y6

25MHZ

1M/F 4

R491

AD16

AC16

220/50V 4

C812

SI

Remove Y6 for AMD recommend

AD11

SATA_X1

AD16

SATA_X2

AC16

220/50V 4

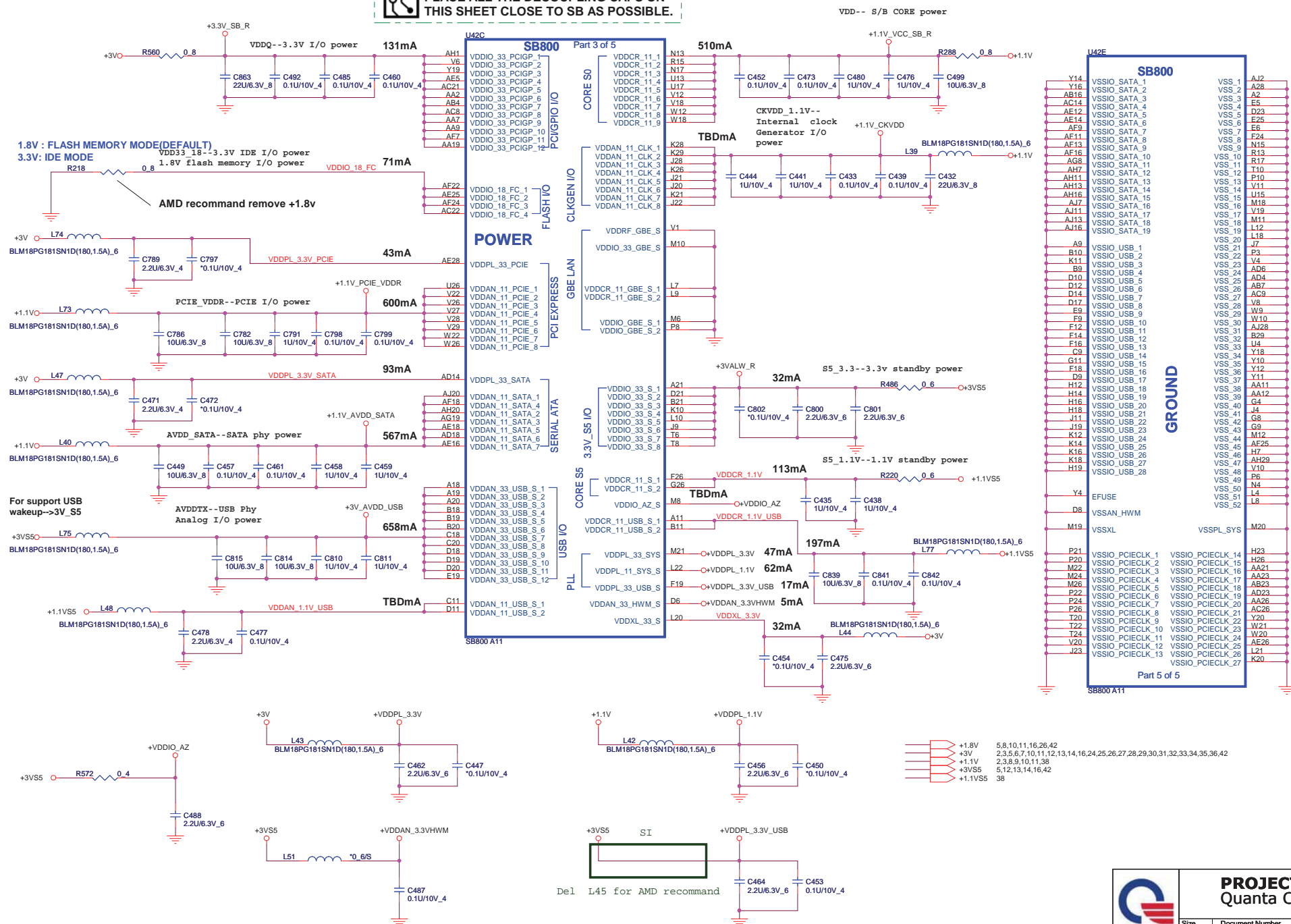
C820

Y6

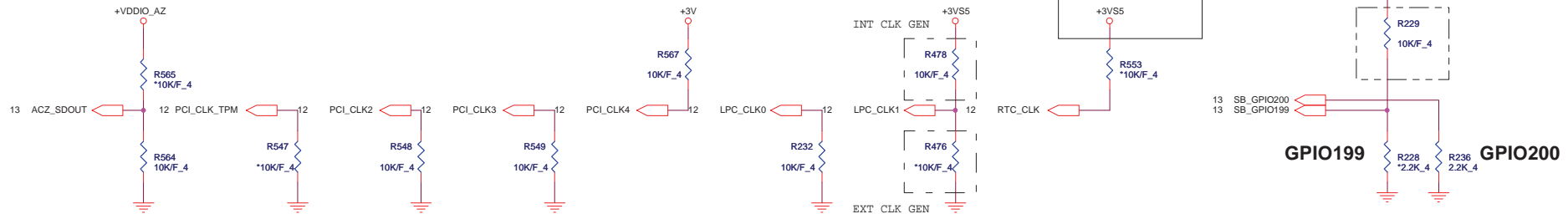
25MHZ

1M/F 4

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



REQUIRED STRAPS



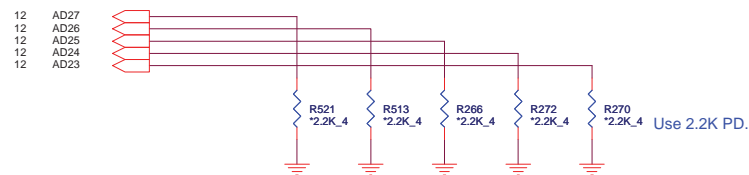
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

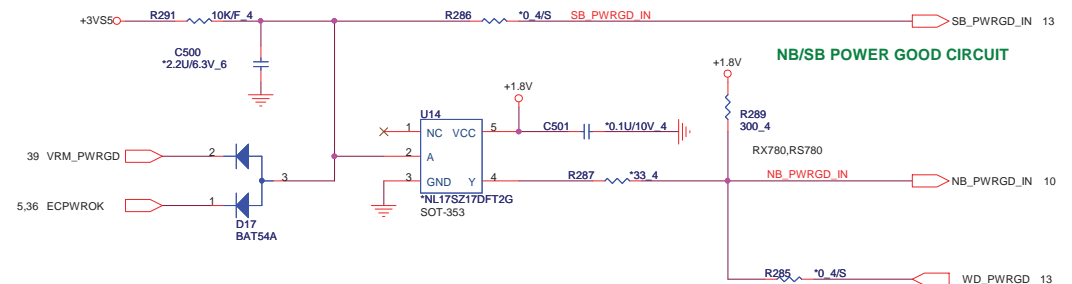
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : LX89
Quanta Computer Inc.

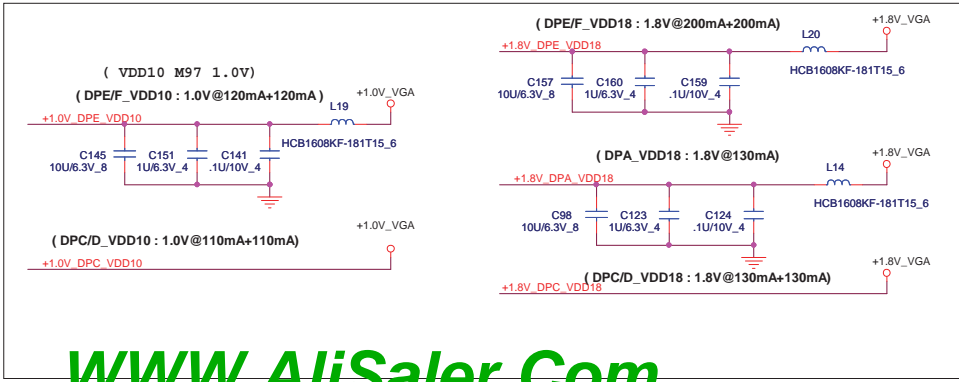
Size Custom

Document Number **SB820-STRAPS**

Date: Monday, September 28, 2009 Sheet 16 of 46

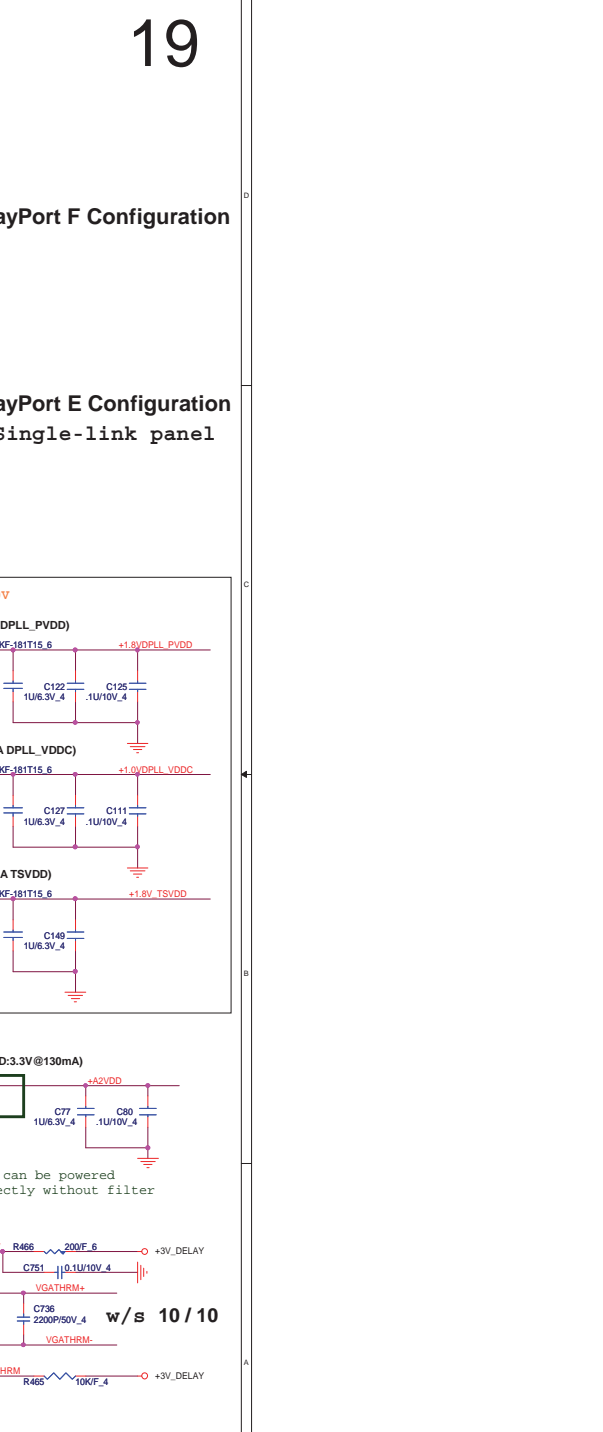
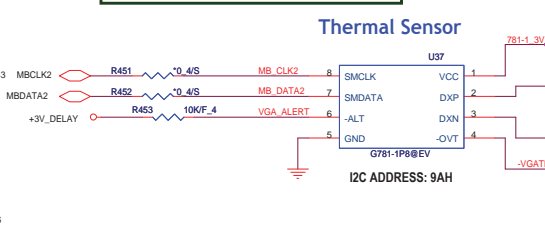
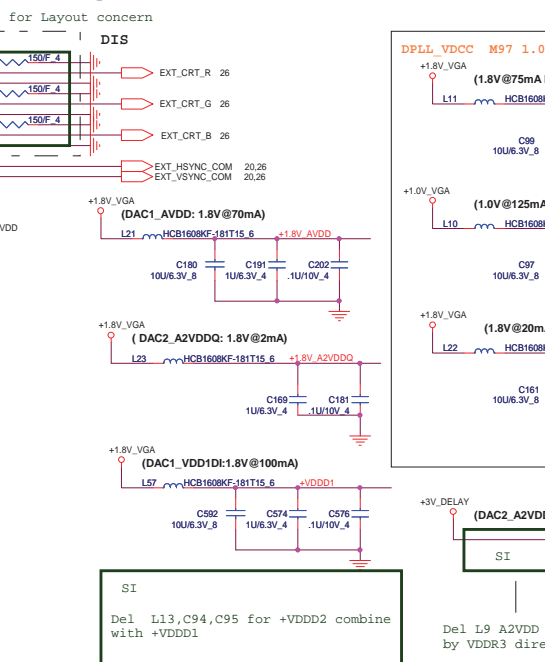
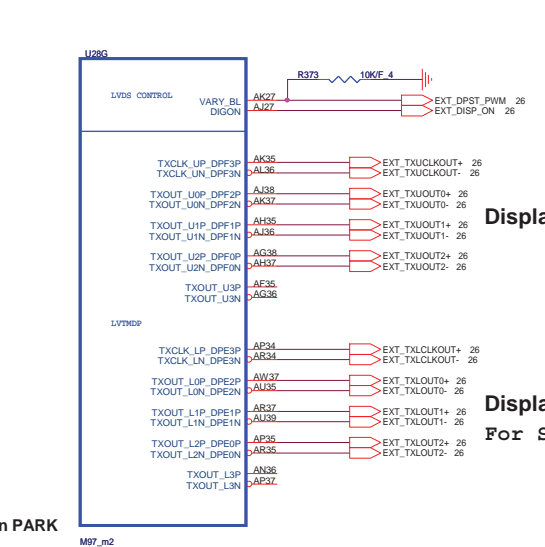
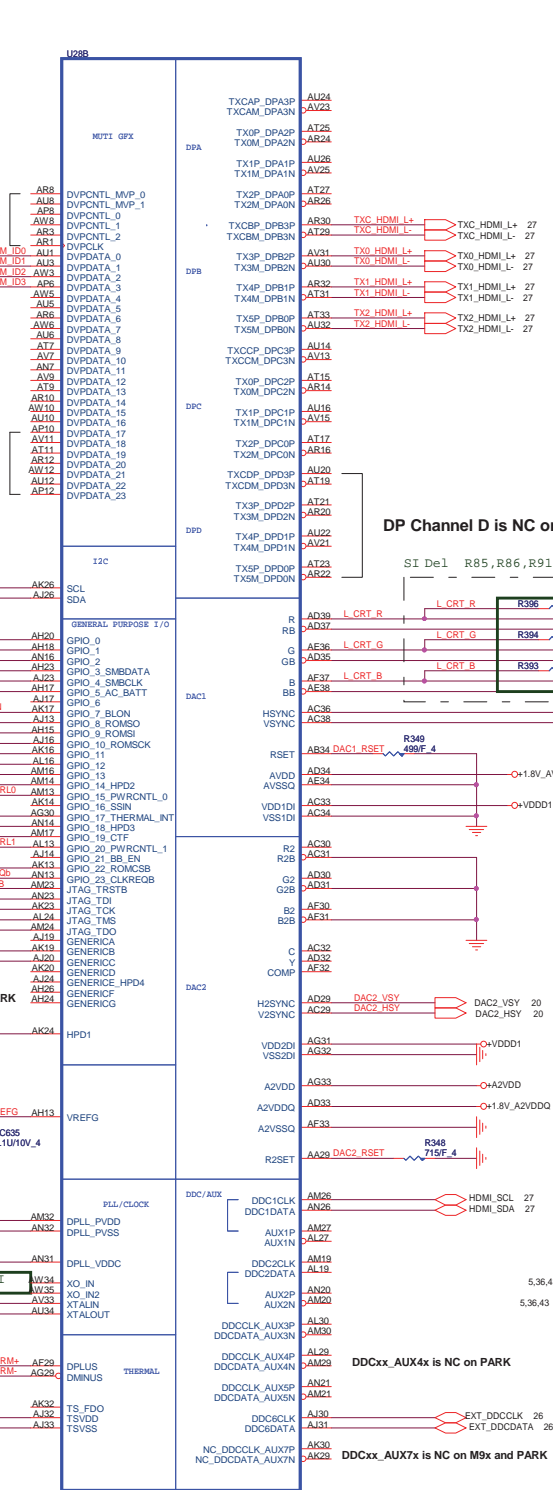
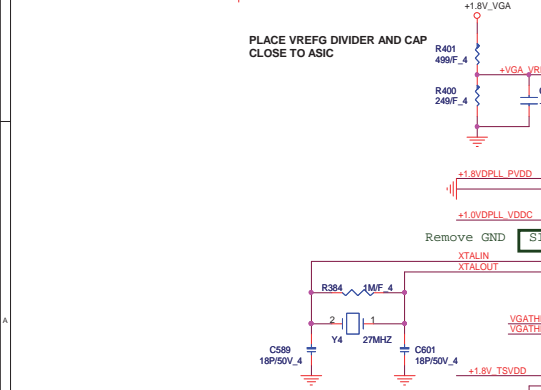
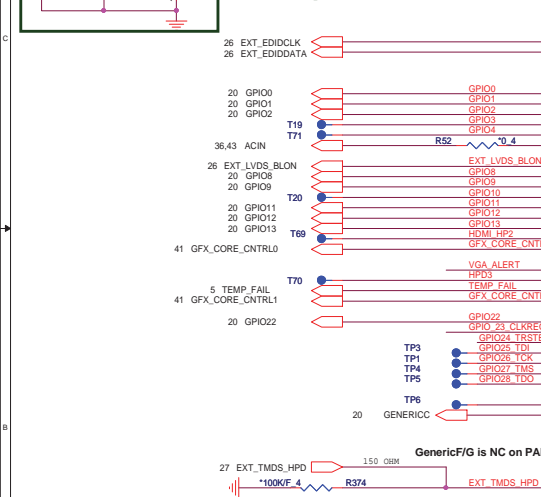
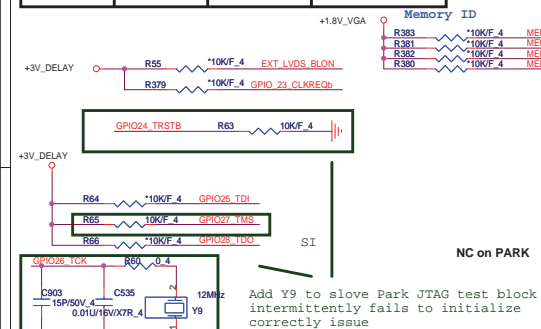
NB5/RD2

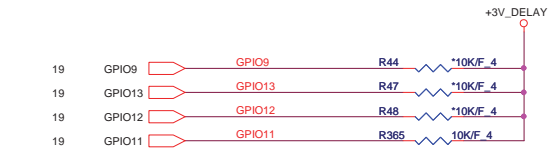
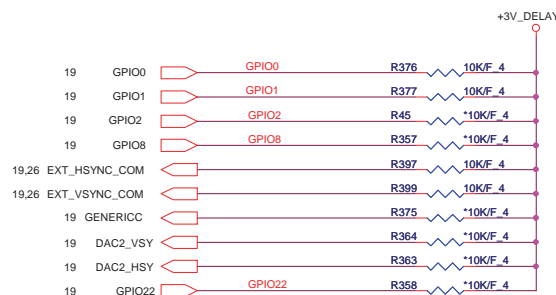
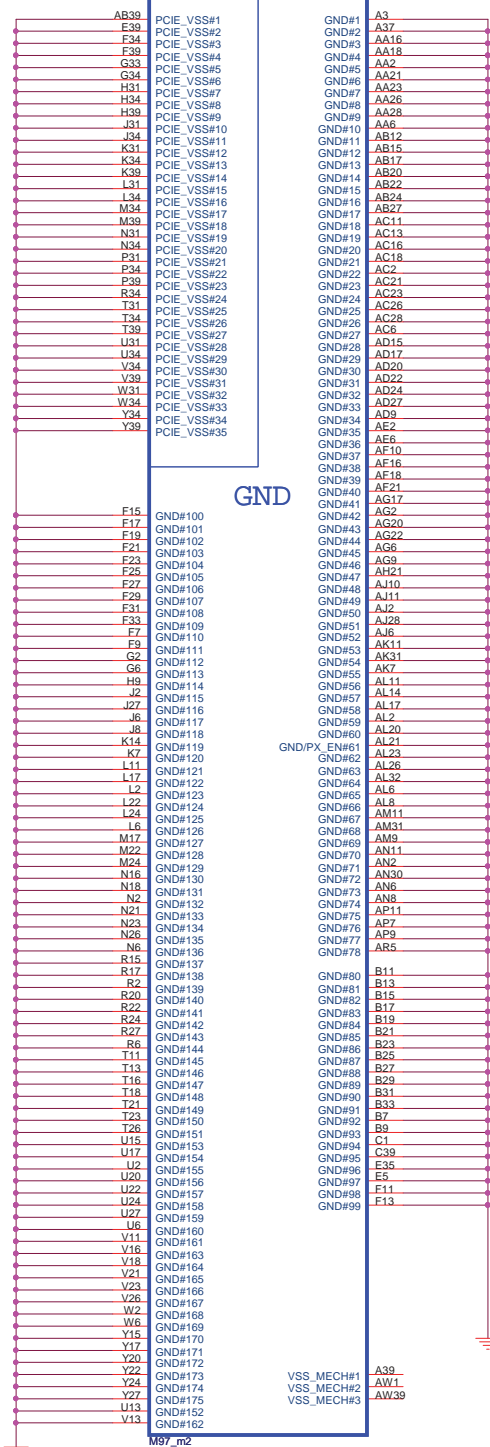
Rev 1A





MEM ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	KAWG1G1645E-HC12
0001	Hynix	64*16-800MHZ	HTS1QG63BF-12C
0010			Reserved
0011			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved





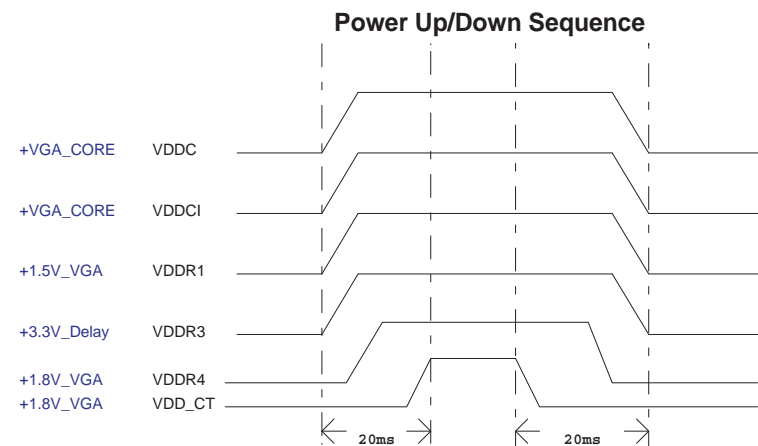
Memory Aperture size fix 256M

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

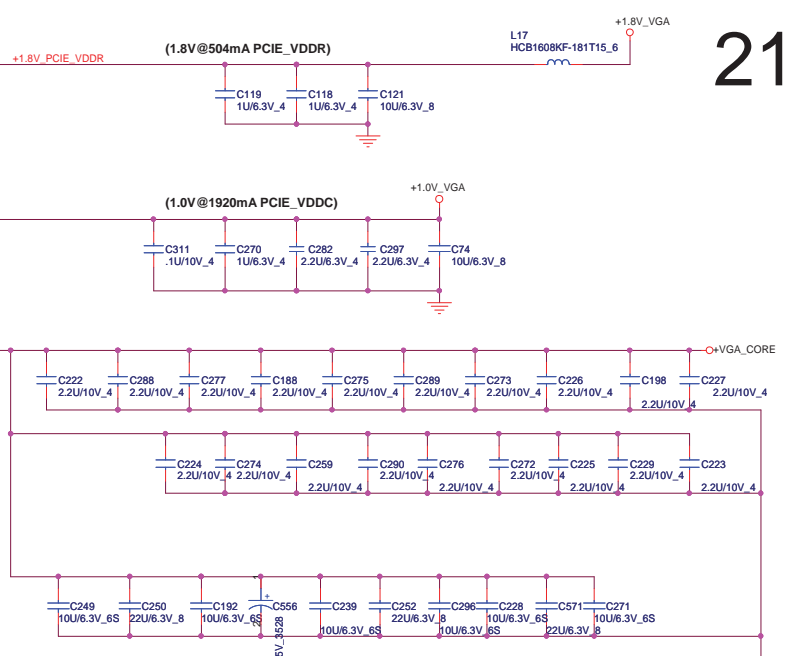
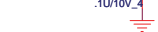
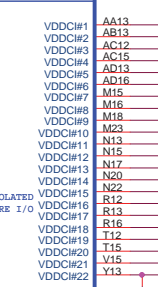
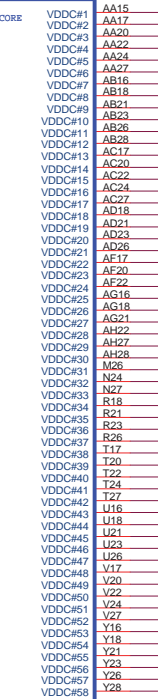
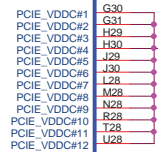
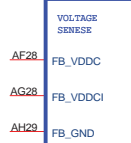
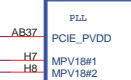
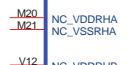
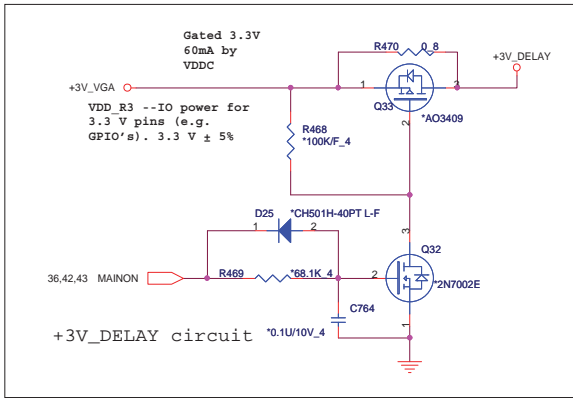
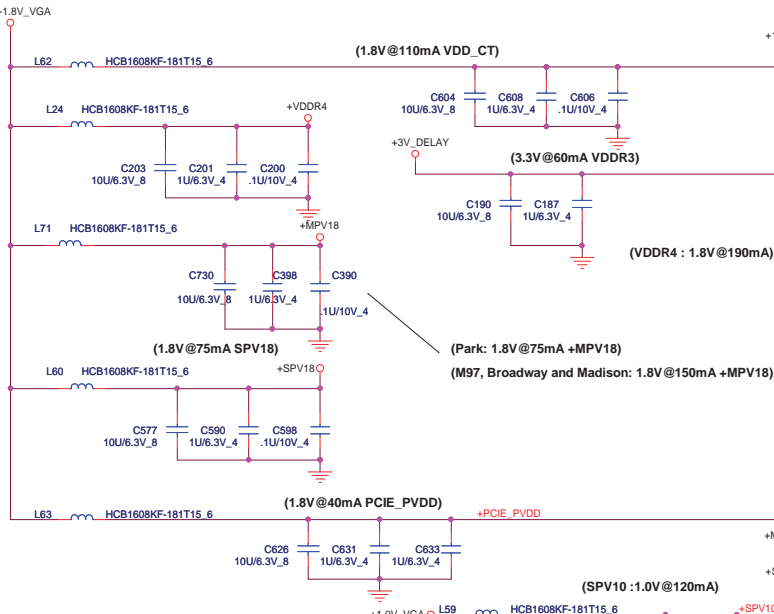
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

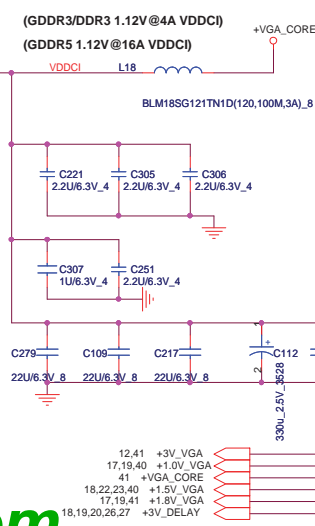
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

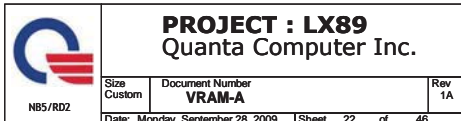


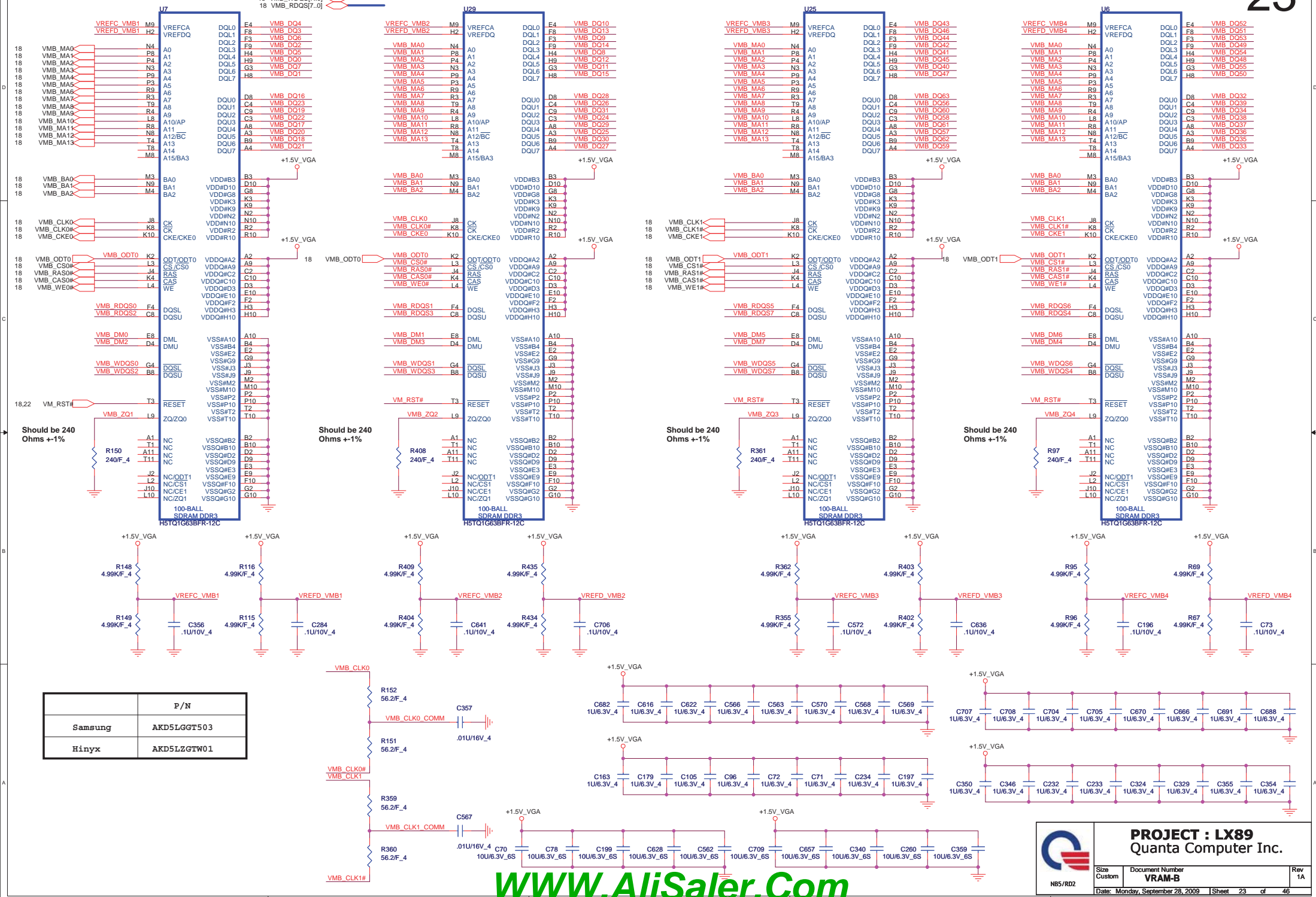
	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom	Rev 1A
Document Number	ATI Park/Madison(GND&Str&Ther)4/5	Date: Monday, September 28, 2009
Sheet 20 of 46		



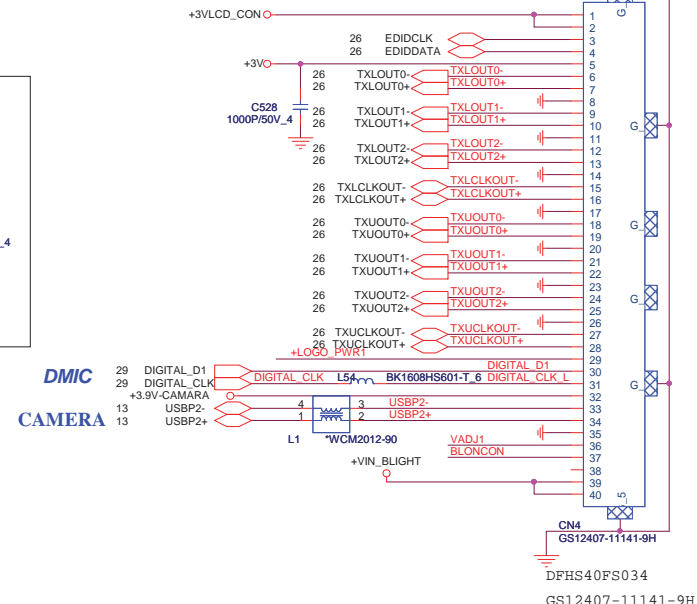
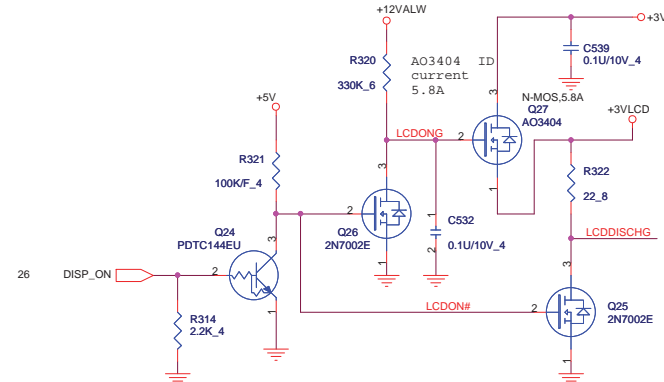
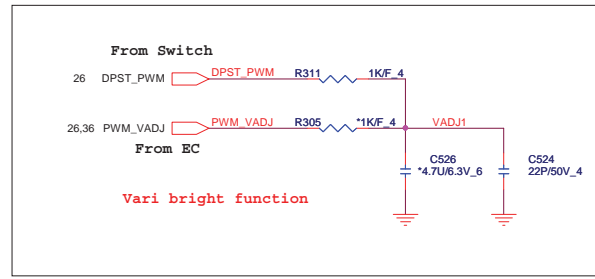
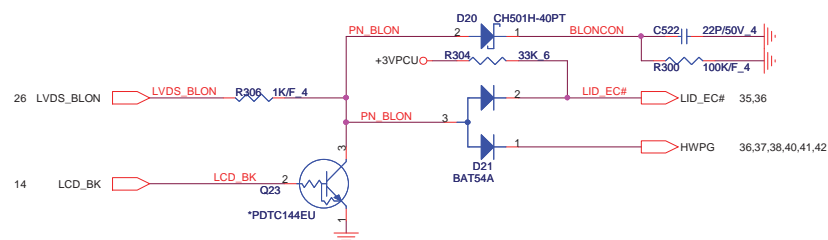
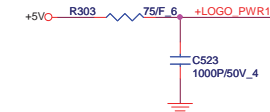
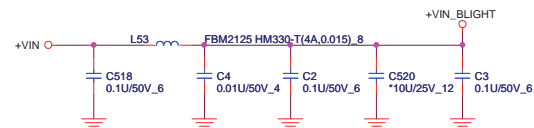
For Madison and Park, VDDCI and VDDC can share one common regulator



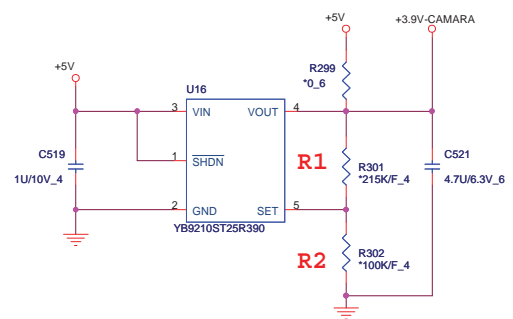




+VIN 31,32,33,39,40,41,42,43
+12VALW 33,35,40,41,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY 18,19,20,21,26,27
+5V 25,26,27,28,29,33,34,35,42

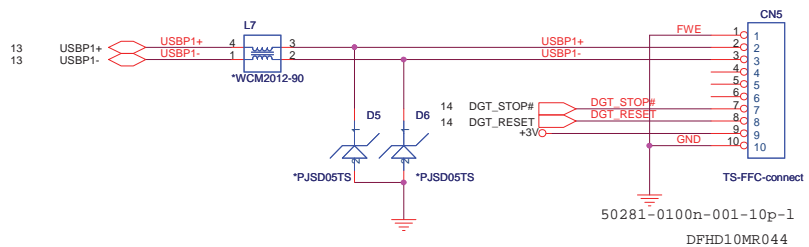


CAMERA POWER



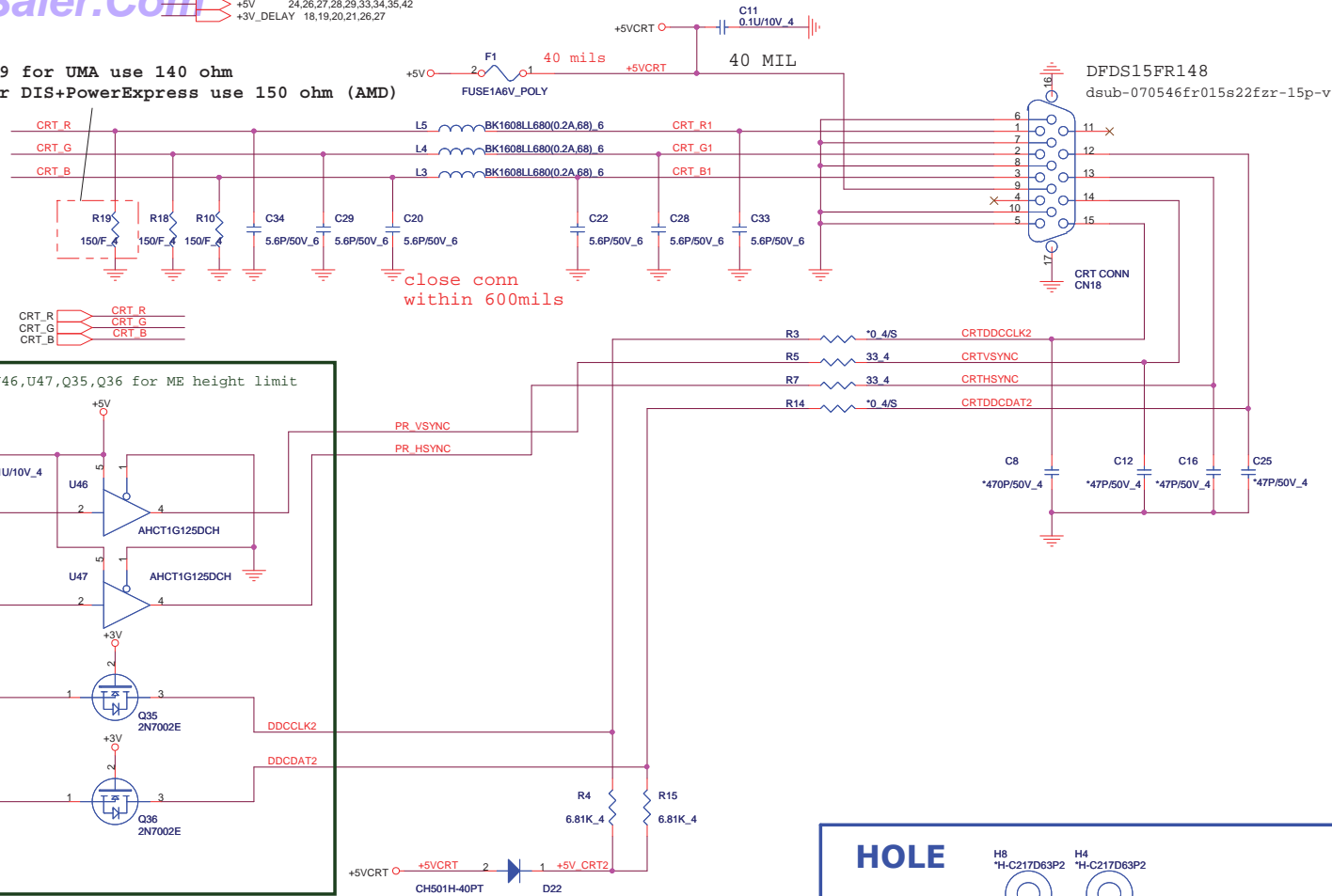
$$V_{out} = 1.25 (1 + R1/R2)$$

Digitizer Connector



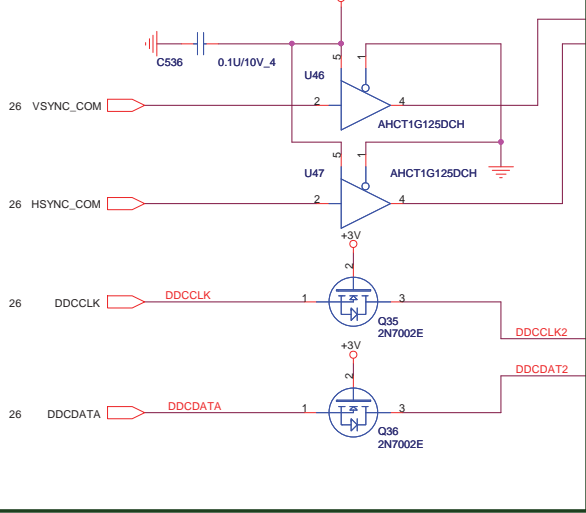
	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom Document Number LCD CONN Date: Monday, September 28, 2009	Sheet 24 of 46	Rev 1A

R19 for UMA use 140 ohm
for DIS+PowerExpress use 150 ohm (AMD)

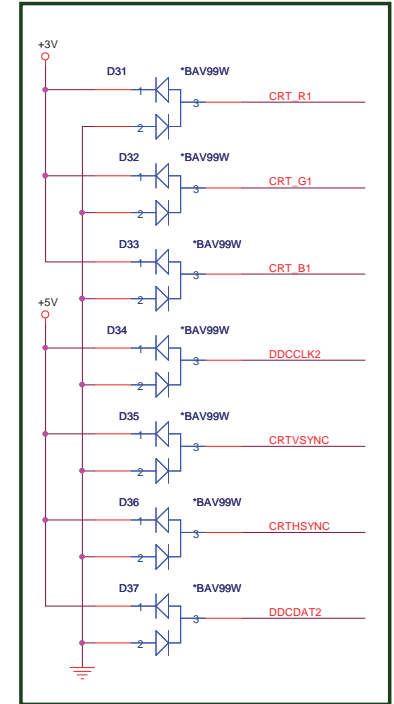


26 CRT_R
26 CRT_G
26 CRT_B

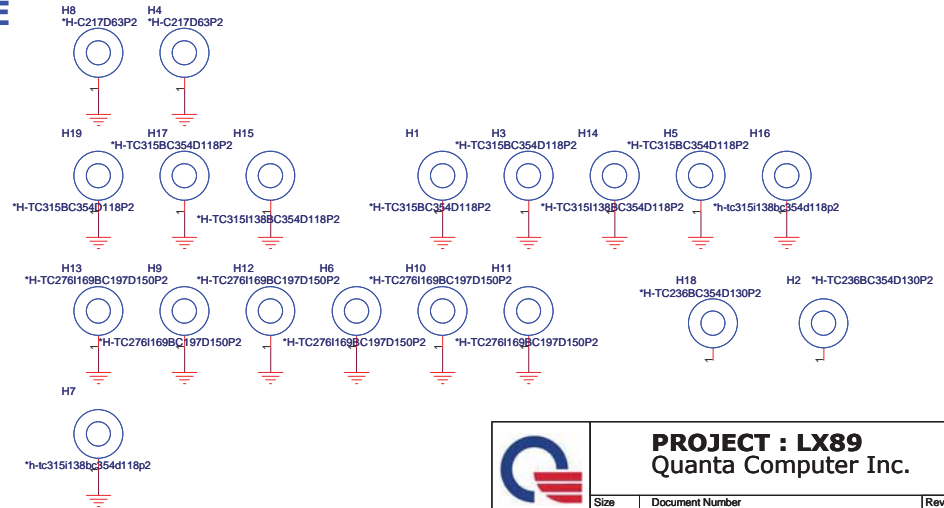
Del U19,C534,C535 add U46,U47,Q35,Q36 for ME height limit
SI




SI Add D31-D37 for ME height limit

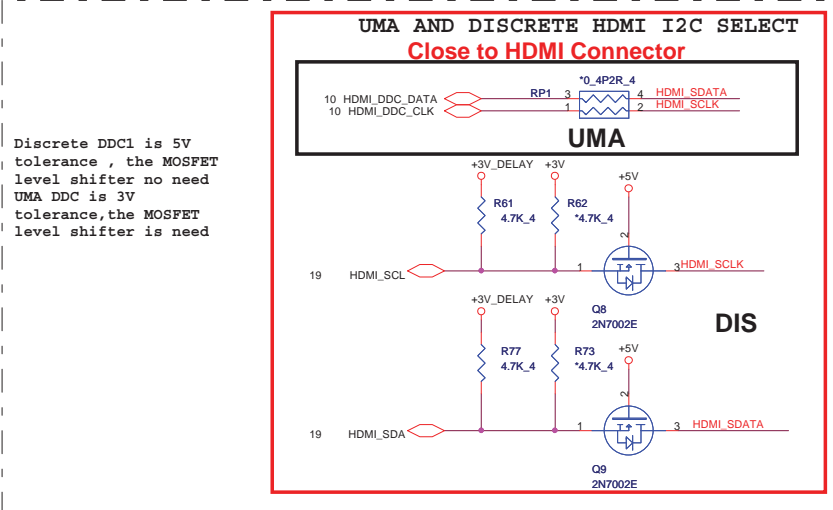
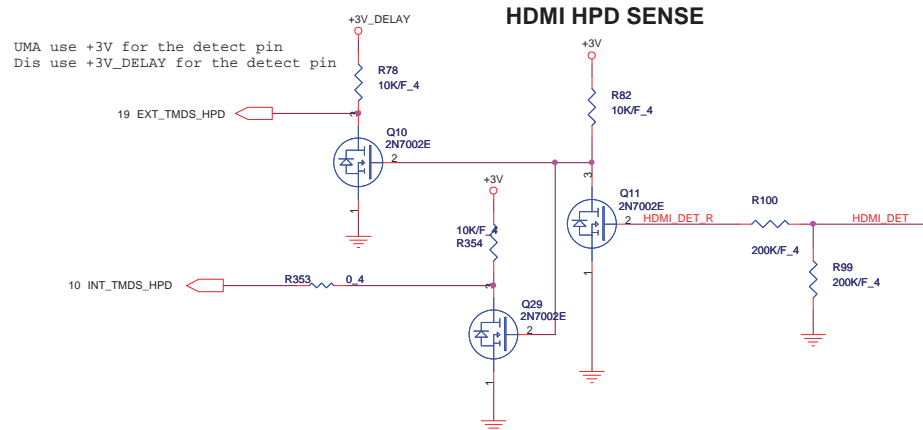
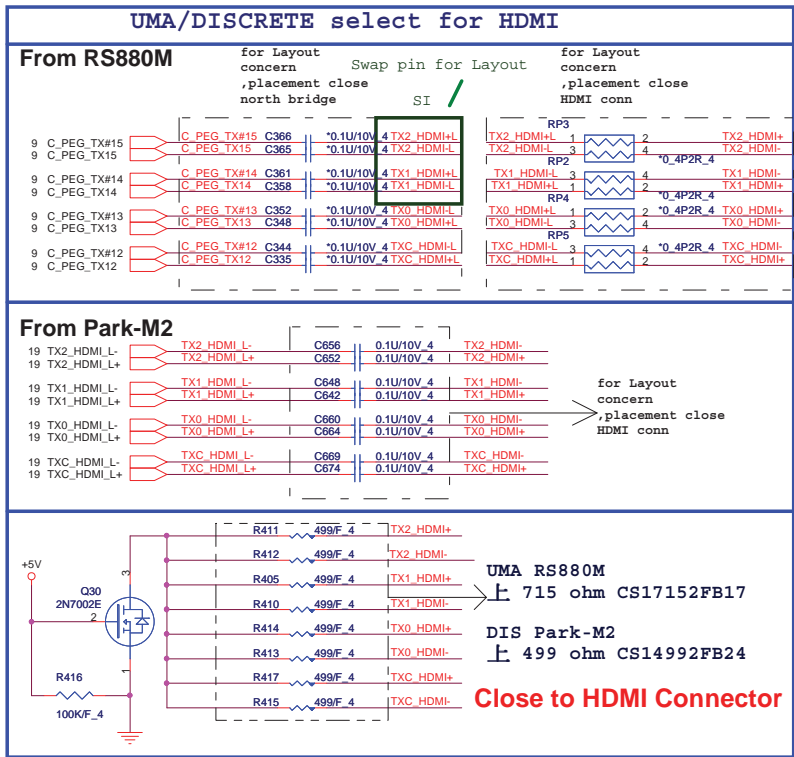


HOLE

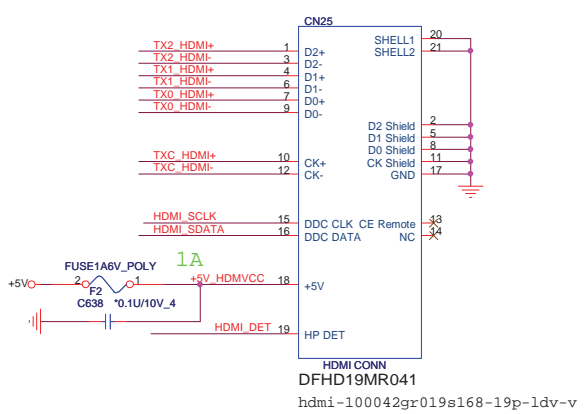
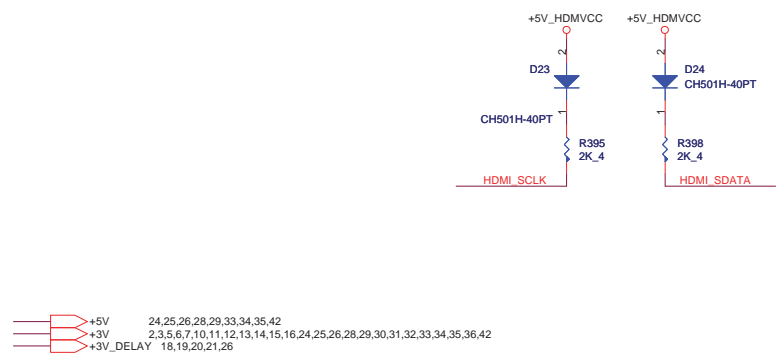


			PROJECT : LX89 Quanta Computer Inc.	
Size Custom	Document Number CRT&HOLE	Rev 1A		
Date: Monday, September 28, 2009	Sheet 25	of 46		



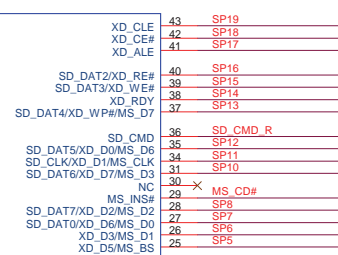
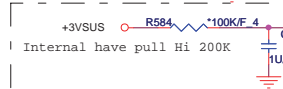
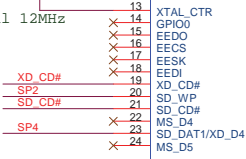
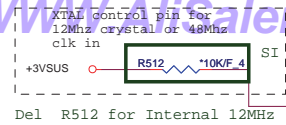


HDMI PORT



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
HDMI		
Date: Monday, September 28, 2009 Sheet 27 of 46		

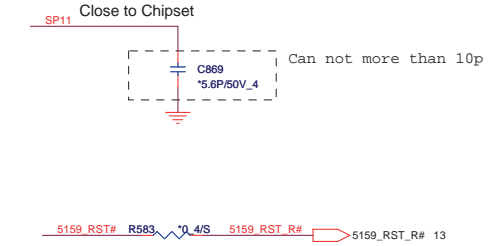


AL005159B00 -->RTS5159GR

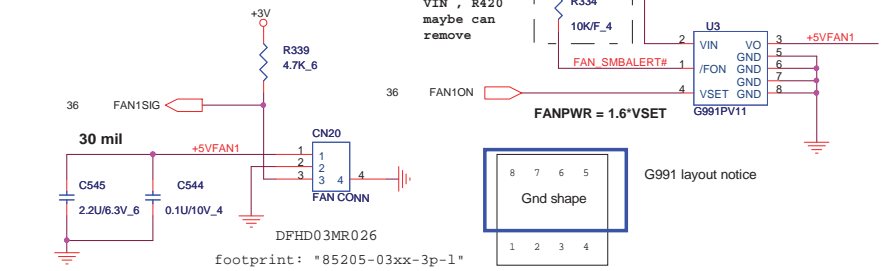
Note:

SD/MMC	MS	XD
SP1	SD_WP	XD_CD#
SP2	SD_CD#	
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5	MS_BS	XD D5
SP6	MS_D1	XD D3
SP7	SD DAT0	MS D0
SP8	SD DAT7	MS D2
SP9	MS_IN#	XD D7
SP10	SD DAT6	MS D3
SP11	SD CLK	MS SCLK
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14	SD DAT3	XD WE#
SP15	SD DAT2	XD RE#
SP16	SD DAT2	XD ALE
SP17	SD DAT2	XD CE#
SP18	SD DAT2	XD CLE
SP19	SD DAT2	XD CLE

SP7	R528	0.4	MS-D0	SD-D0	XD-D6
SP6	R524	0.4	MS-D1	XD-D3	SD-D1
SP8	R531	0.4	MS-D2	XD-D2	
SP16	R579	0.4	XD-RE#	SD-D2	
SP5	R522	0.4	MS-BS	XD-D5	
SP15	R578	0.4	SD-D3	XD-WE	
SP11	R569	0.4	SD CLK	MS_CLK	
SP2	R511	0.4	SD_WP		
SP13	R576	0.4	XD-WP#		
SP19	R582	0.4	XD-CLE		
SP4	R510	0.4	XD-D4		
SP10	R537	0.4	MS-D3	XD-D7	
SP14	R577	0.4	XD-RB#		
SP12	R570	0.4	XD-D0		
SP17	R580	0.4	XD-ALE		
SP18	R581	0.4	XD-CE#		
SD_CMD_R	R571	0.4	SD-CMD		



CPU FAN

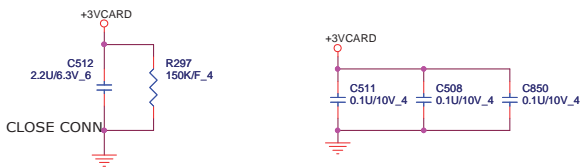


5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/XD Cards

DFHD36MR005

4in1-cm4s-125-36p-r-v



PROJECT : LX89
Quanta Computer Inc.

Size Custom

Document Number **RTS5159&CPU FAN**

Rev 1A

Date: Monday, September 28, 2009

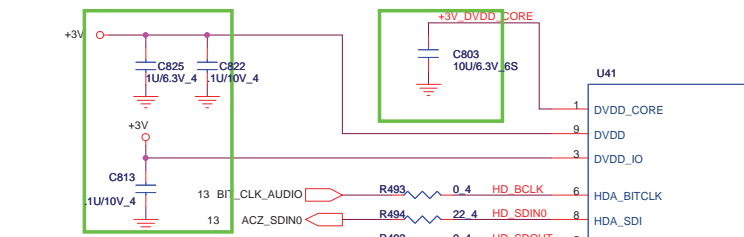
Sheet 28 of 46

NBS/RD2

2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,30,31,32,33,34,35,36,42
+3V
+5V

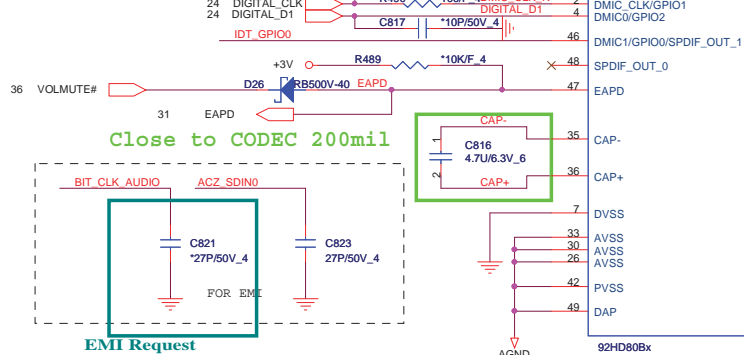
Close to CODEC 200mil

Close to CODEC 200mil

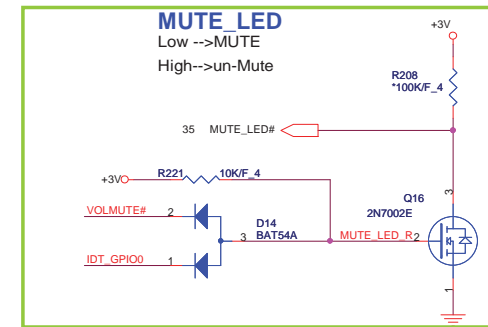


HDA Bus

TO Digital MIC



EMI Request



MUTE_LED

Low -->MUTE
High-->un-Mute



Change P/N to AL80B1X5001

TO Audio Jack MIC

TO Headphone jack

TO Internal Speakers

TO Internal Speakers

TO Internal Speakers

TO Internal Speakers

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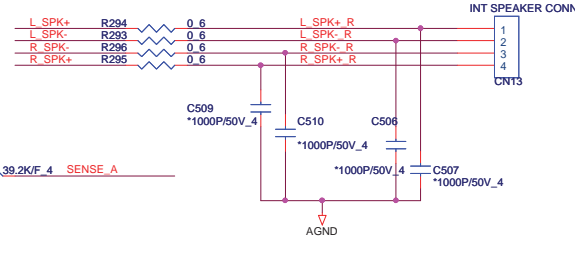
PLACE CLOSE TO PIN 13,14 within 500mil

Changed by IDT recommend

Close to CODEC 200mil

INT. SPEAKER

H=2.0 footprint: "3800-X04N-00X-4P-L"
DFHD04MR142

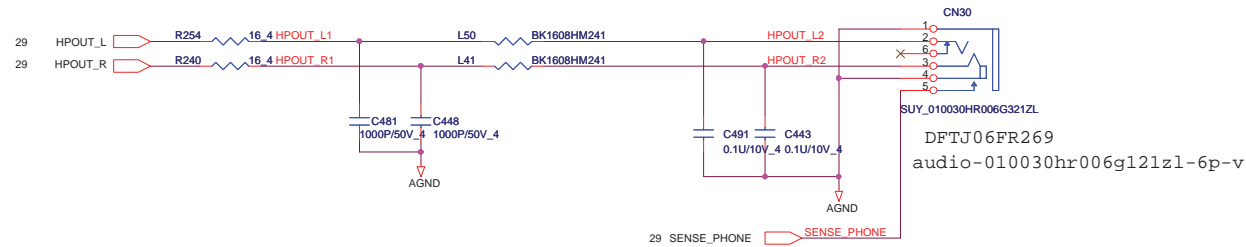


	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number Azalia 92HD80	Rev 1A
NBS/RD2	Date: Monday, September 28, 2009	Sheet 29	of 46

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

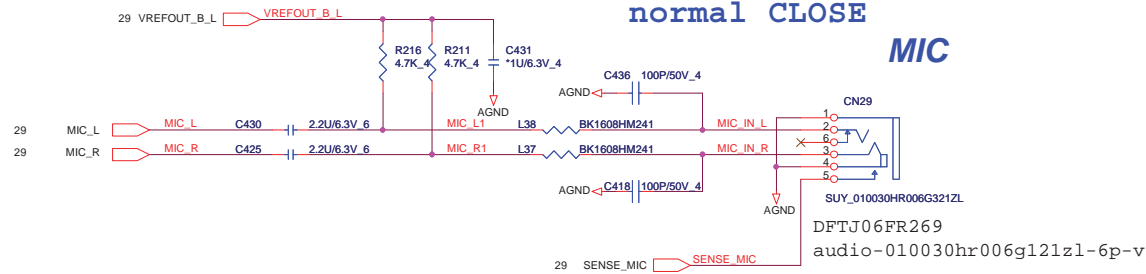
33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

normal CLOSE Line out



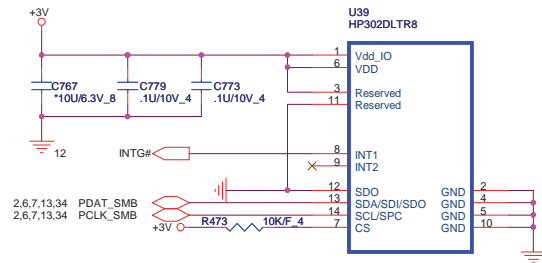
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.


normal CLOSE MIC



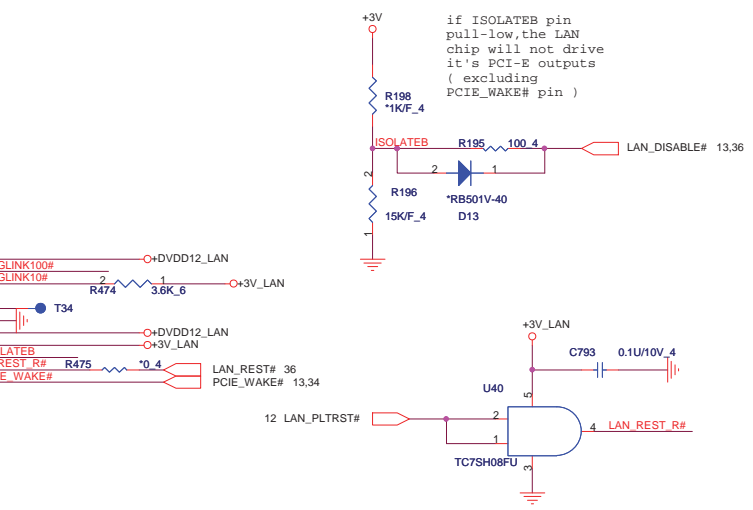
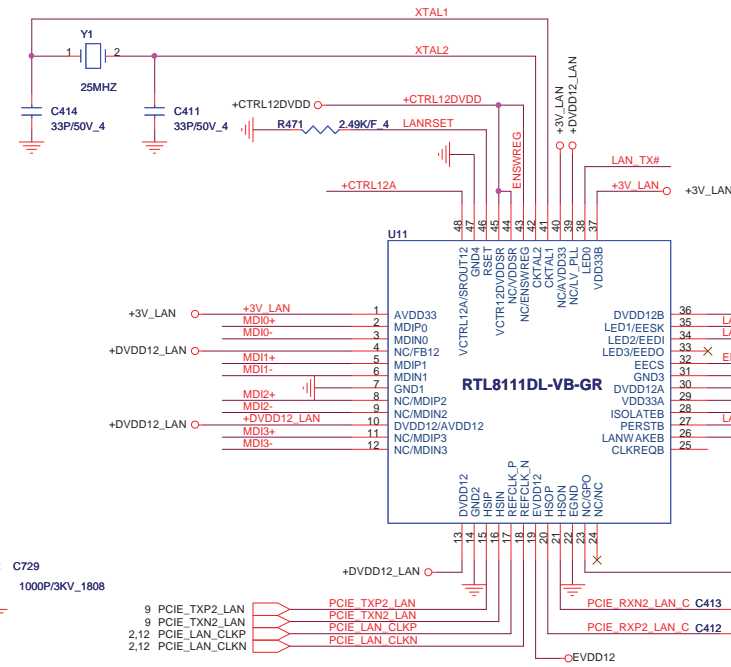
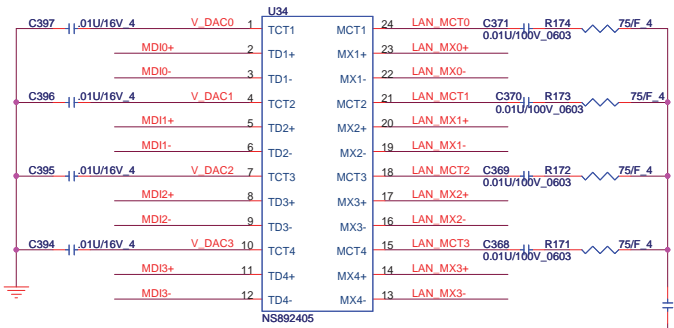
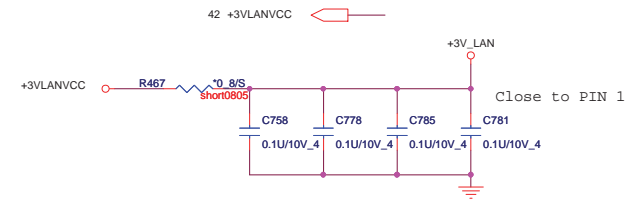
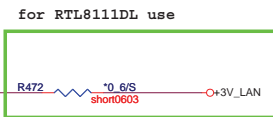
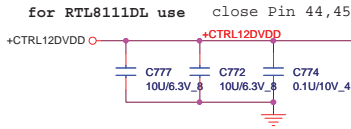
Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low

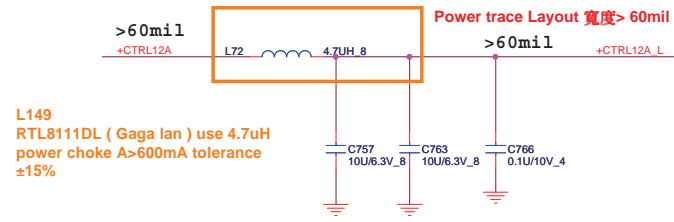


 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.			Rev 1A
	Size Custom	Document Number Audio Jack/Accelerometer		
	Date: Monday, September 28, 2009 Sheet 30 of 46			

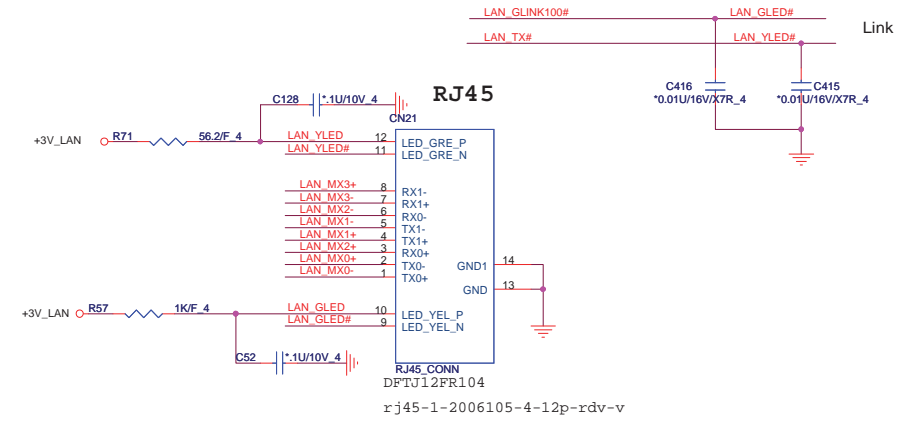
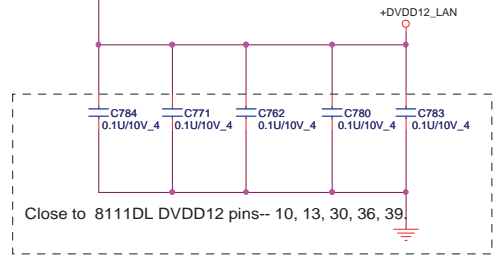
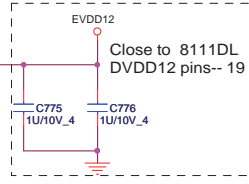
T : Stuffed for RTL8111DL(10/100/1000)



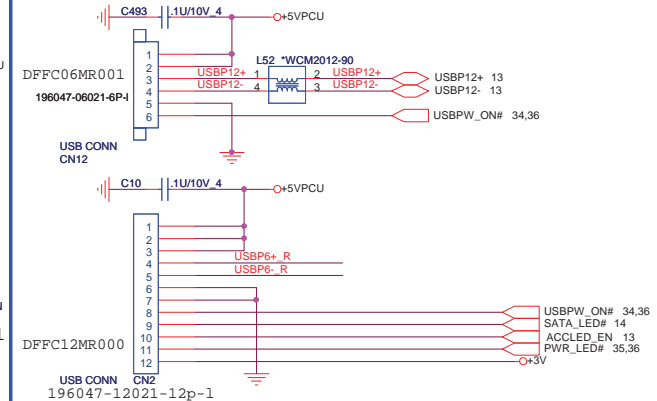
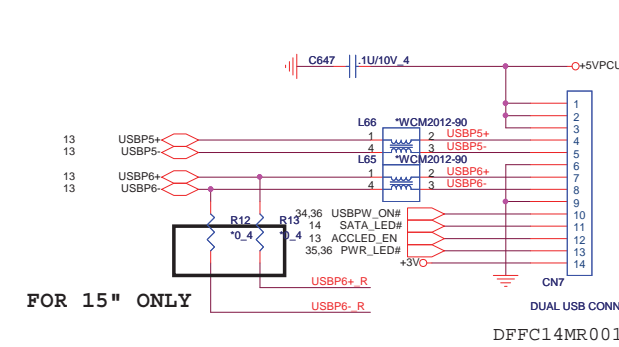
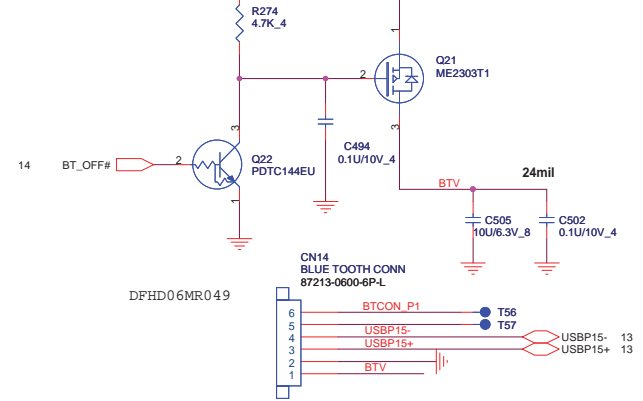
NS892402:GIGABIT DB0AT9LAN05



L149
RTL8111DL (Giga lan) use 4.7uH
power choke A>600mA tolerance
±15%

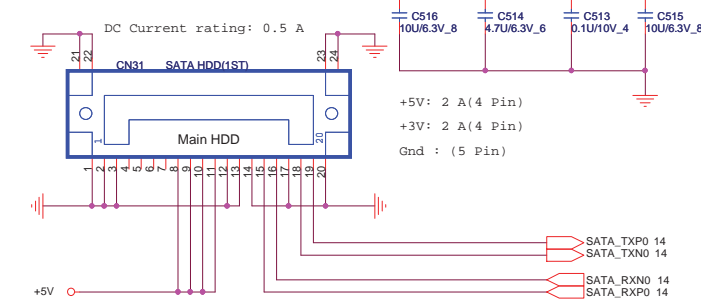


	PROJECT : LX89		
	Quanta Computer Inc.		
	Size Custom	Document Number RTL8111DL/RJ45	Rev 1A
Date: Monday, September 28, 2009		Sheet 32 of 46	



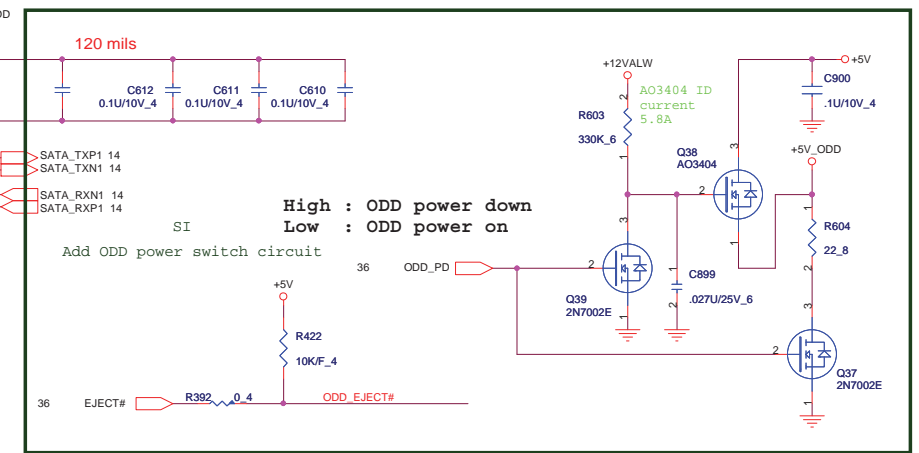
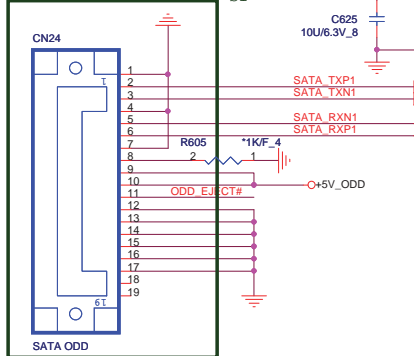
SATA HDD CONNECTOR

H=2.6 Footprint: "GS12201-1011-9F-20P-L"
DFHD20MR023



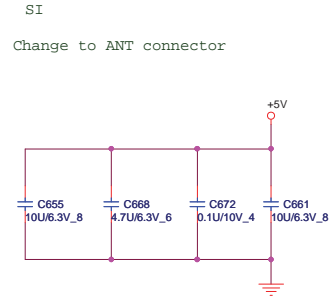
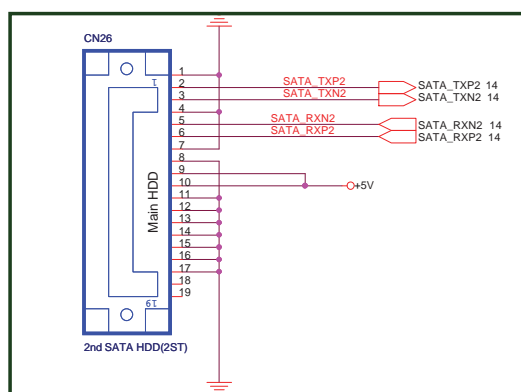
SATA CD-ROM

Change to ANT connector



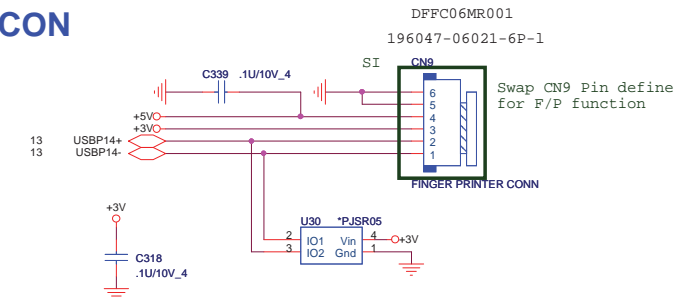
SATA_2 HDD CONNECTOR FOR 17.3"

+5V: 2 A(4 Pin)
Gnd : (5 Pin)



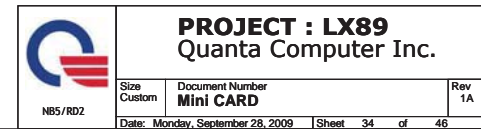
USB Fingerprint CON

1. SYSTEM GND
2. SYSTEM GND
3. LED PWR(+5V)
4. USB PWR(+3V)
5. USB1.1+
6. USB1.1-

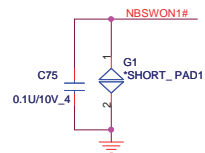


PROJECT : LX89
Quanta Computer Inc.

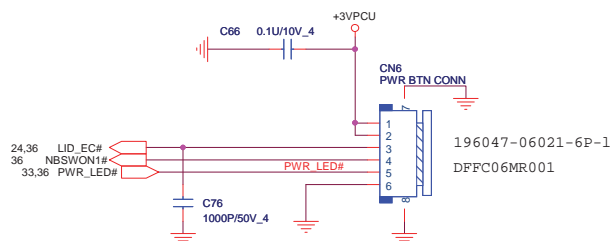
Size Custom	Document Number BT/FP/USBX2/SATA HDDX2/ODD	Rev 1A
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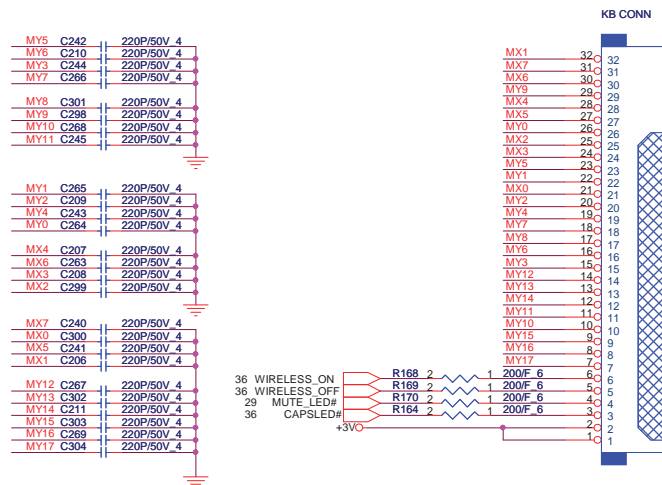
POWER BUTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
- 2.(+3VPCU)
3. LIDSWITCH
- 4.POWERON#
5. PWRLED#
6. GND



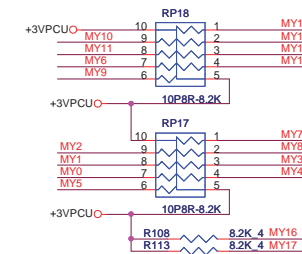
KEYBOARD Con.



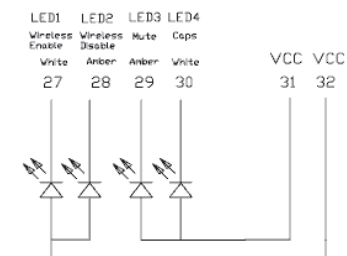
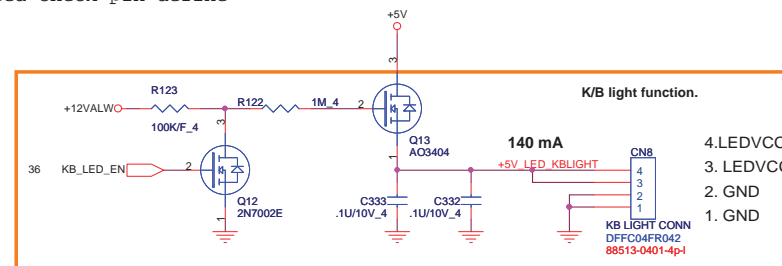
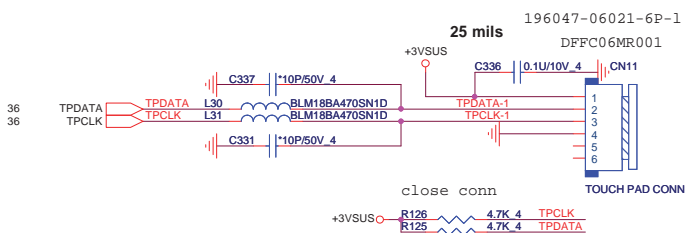
Need check pin define



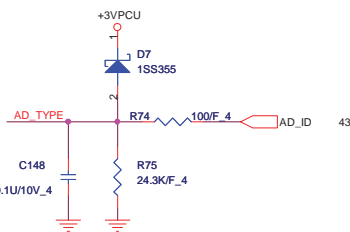
KEYBOARD PULL-UP



TOUCH PAD CONN

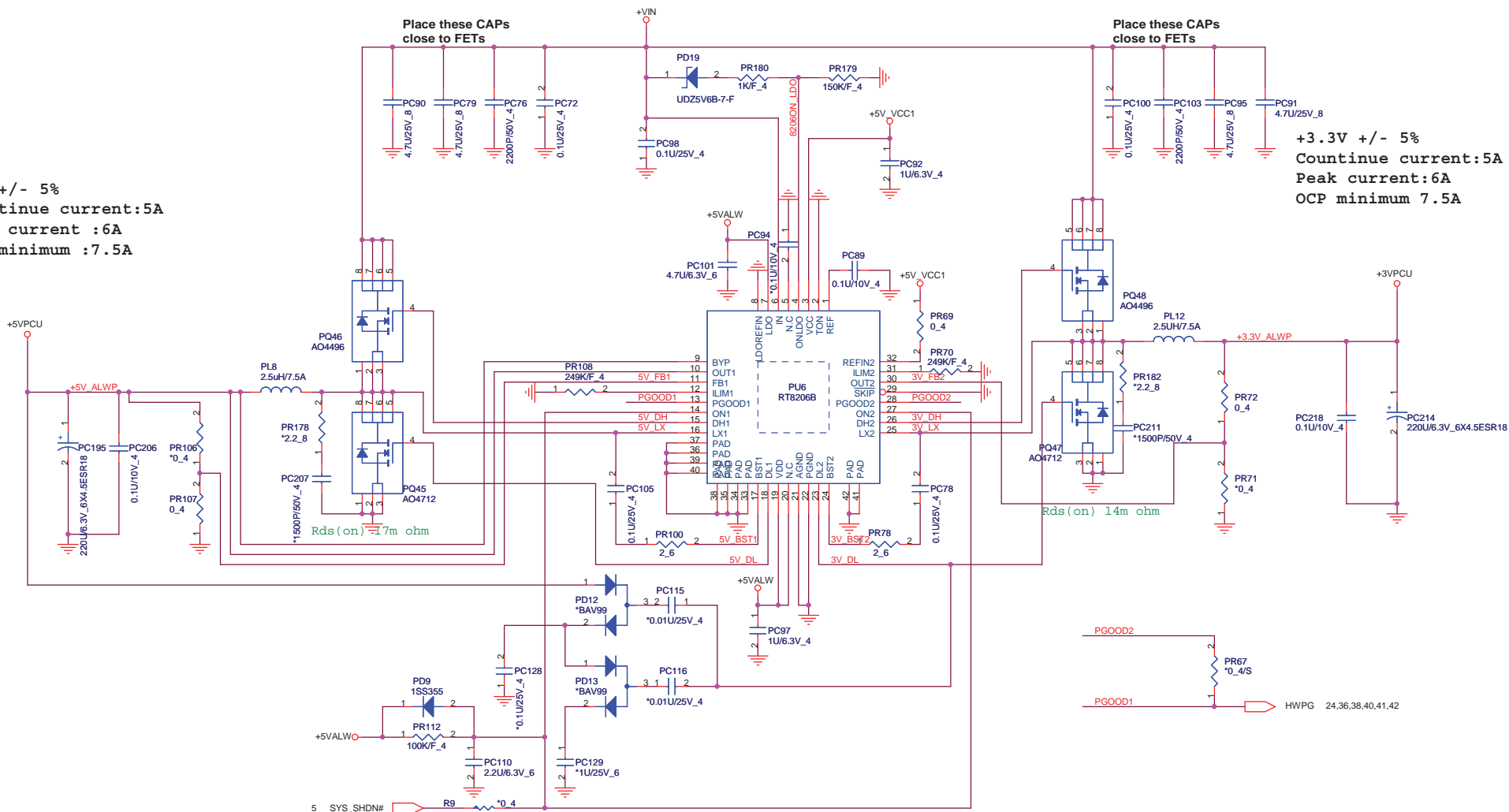


12		30	112		50	119	56		51		13	123		62	126	76	91	94
1		110	115	127	35	118	125		36		41	122	107		15	75	92	95
8	58	16	114		21	117	28		22		27	121			90	80	93	96
9		1	113	70	6	116	45	59	7		12	120	129	29 42	85	101	97	
5	64	31	33	71	34	32	38		37		40	39			43	86	106	104
6		46	48	72	49	47	53		52	44	55	54			61	81	100	103
3		2	4	73	5	3	9		8		11	10		60	84	89	99	102
2		17	19	74	20	18	24		23	57	26	25			83	79	105	108
	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26



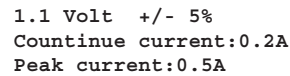
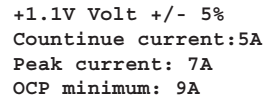
+5V +/- 5%
Countinue current:5A
Peak current :6A
OCP minimum :7.5A

+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A



+VIN 24,31,38,39,40,41,42,43
+3VPCU 4,6,12,24,33,35,36,38,39,40,41,42,43
+5VPCU 33,34,36,38,39,40,41,42,43

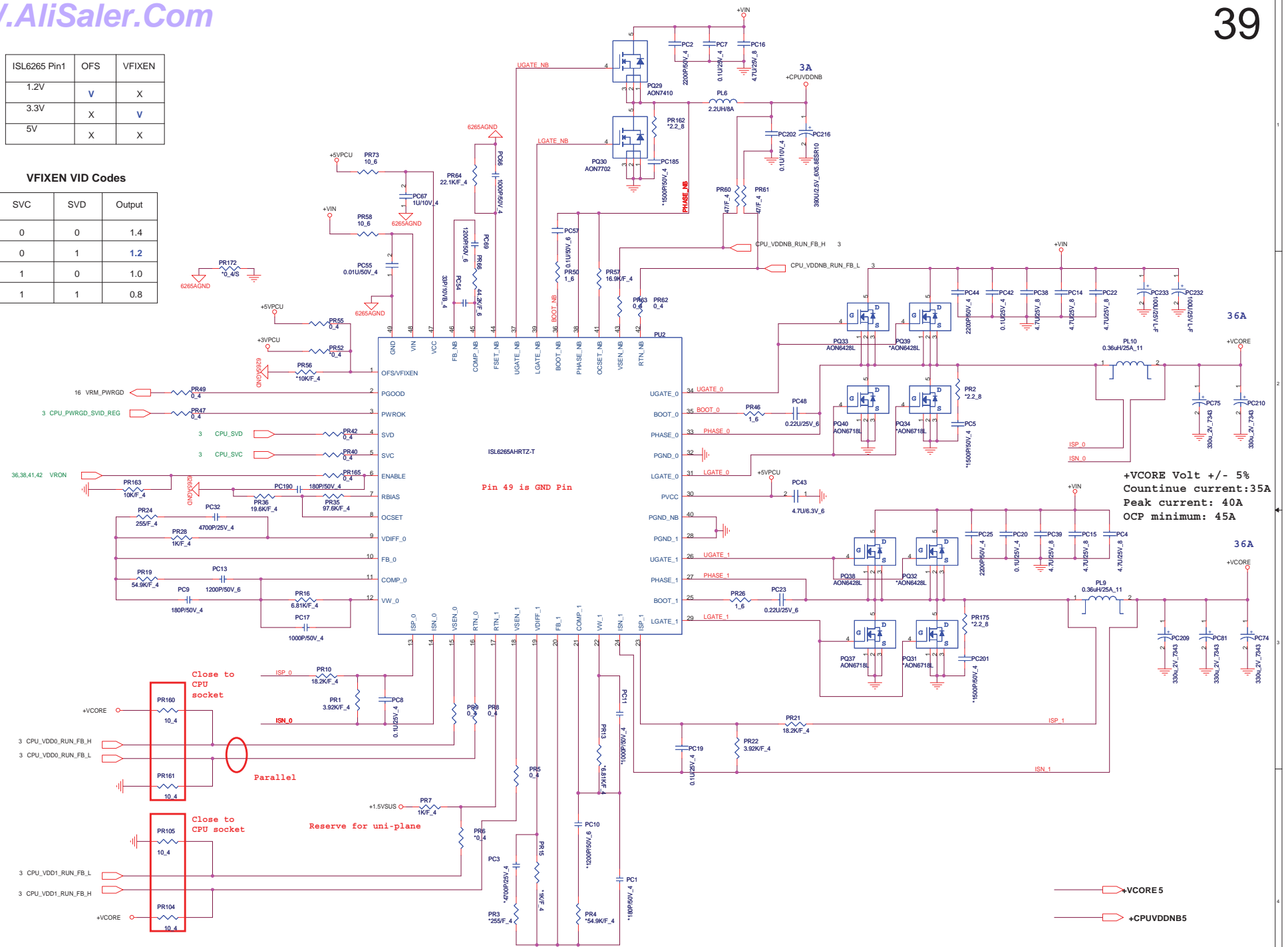
	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Size Custom Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Monday, September 28, 2009 Sheet 37 of 46		

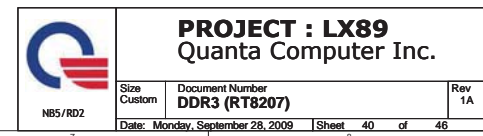


ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

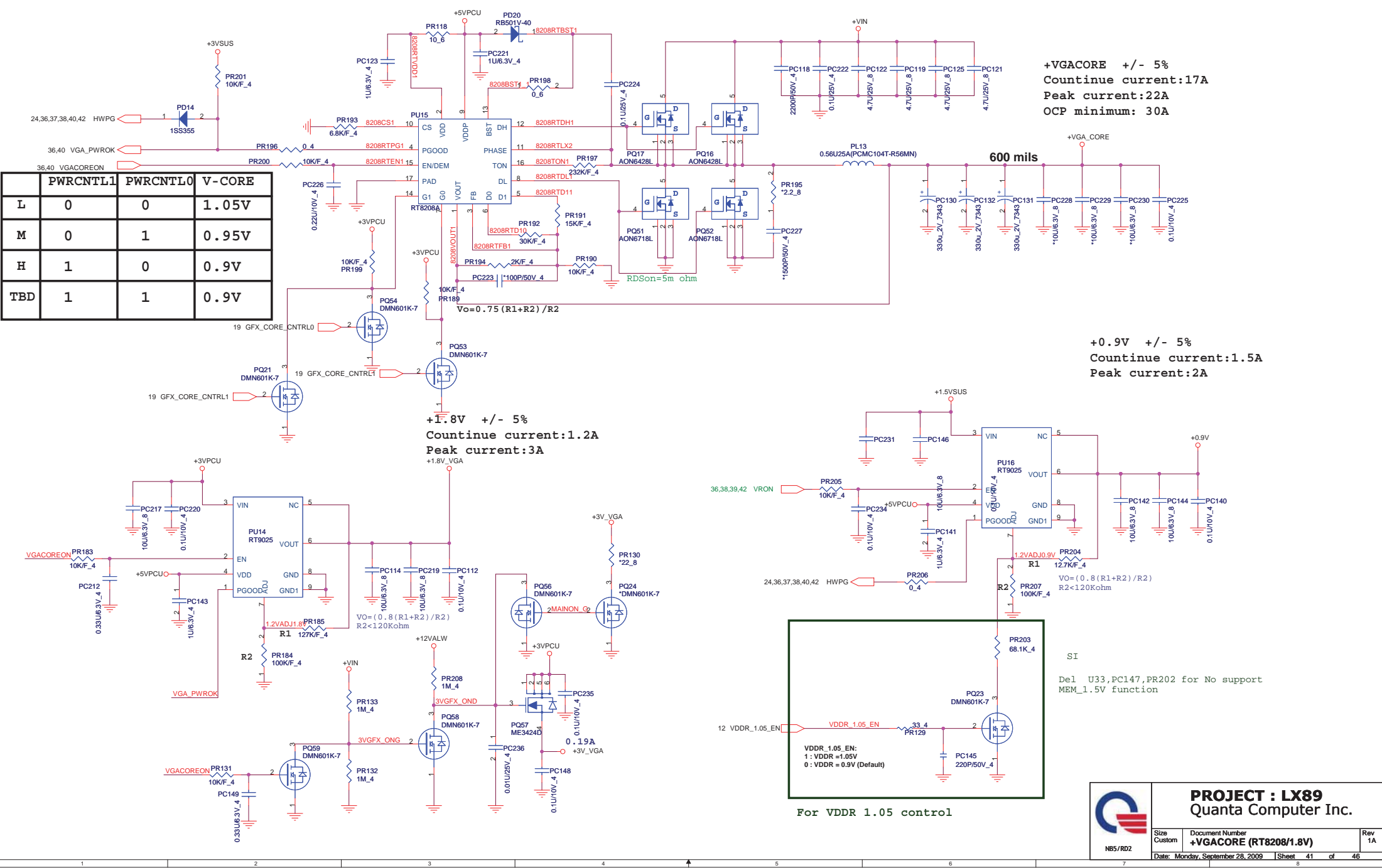
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V



+VGACORE +/- 5%
Countinue current:17A
Peak current:22A
OCP minimum: 30A

+0.9V +/- 5%
Continue current:1.5A
Peak current:2A

VDDP105V_EN

33.4 PR129

68.1K PR203

5V

PQ23 DMN601K-7

2

PC145 220P/50V_4


VDDP105V

VDDP105V_EN: 1: VDDP = 1.05V 0: VDDP = 0.9V (Default)

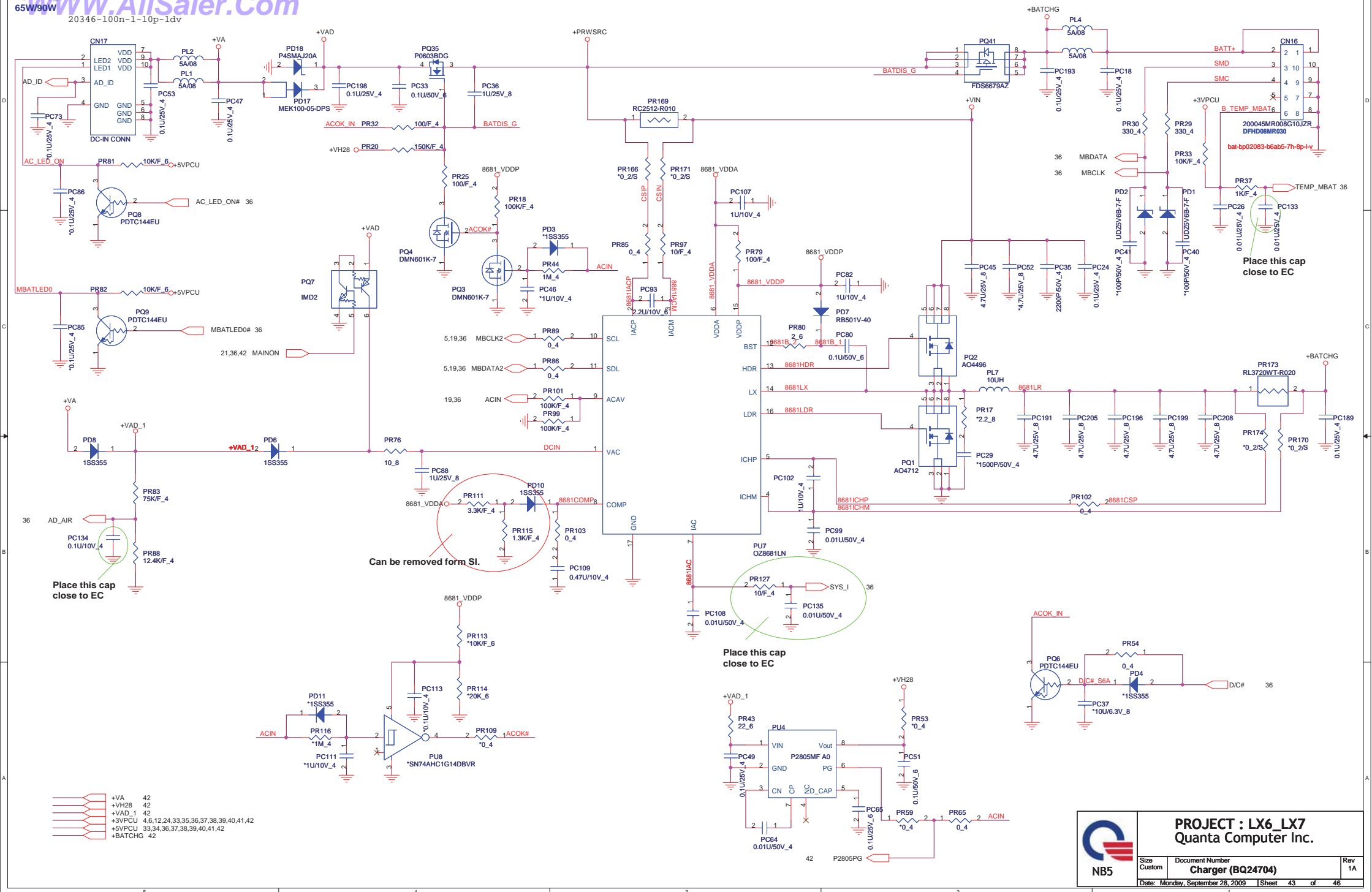
For VDDR 1.05 control

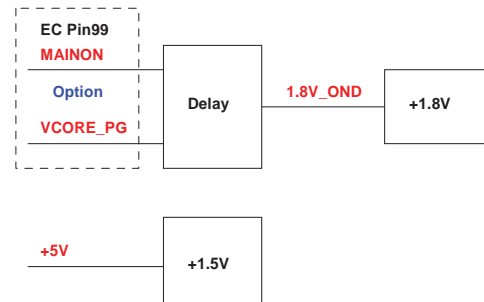
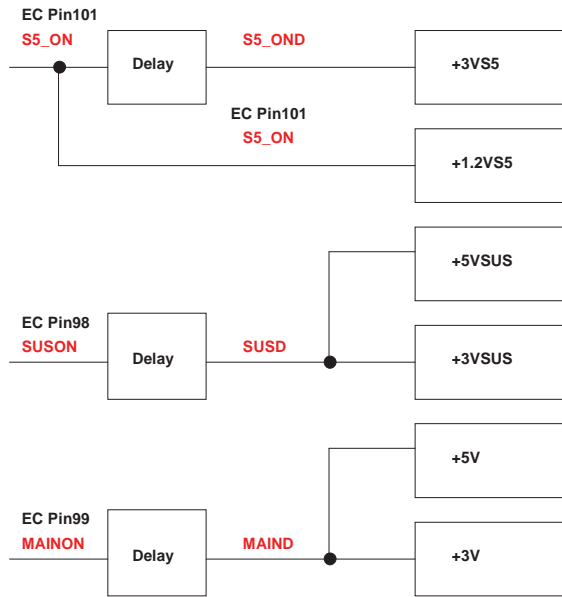
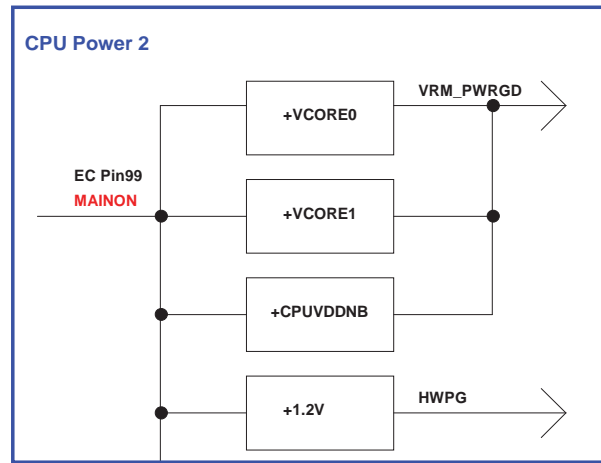
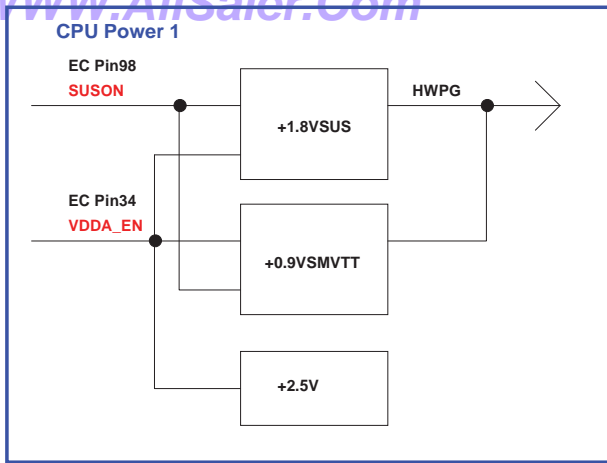
SI

Del U33,PC147,PR202 for No support
MEM_1.5V function

 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev 1A
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Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT